MAINTENANCE PRACTICE

for the

701A/702A

TRANSMISSION TEST SETS

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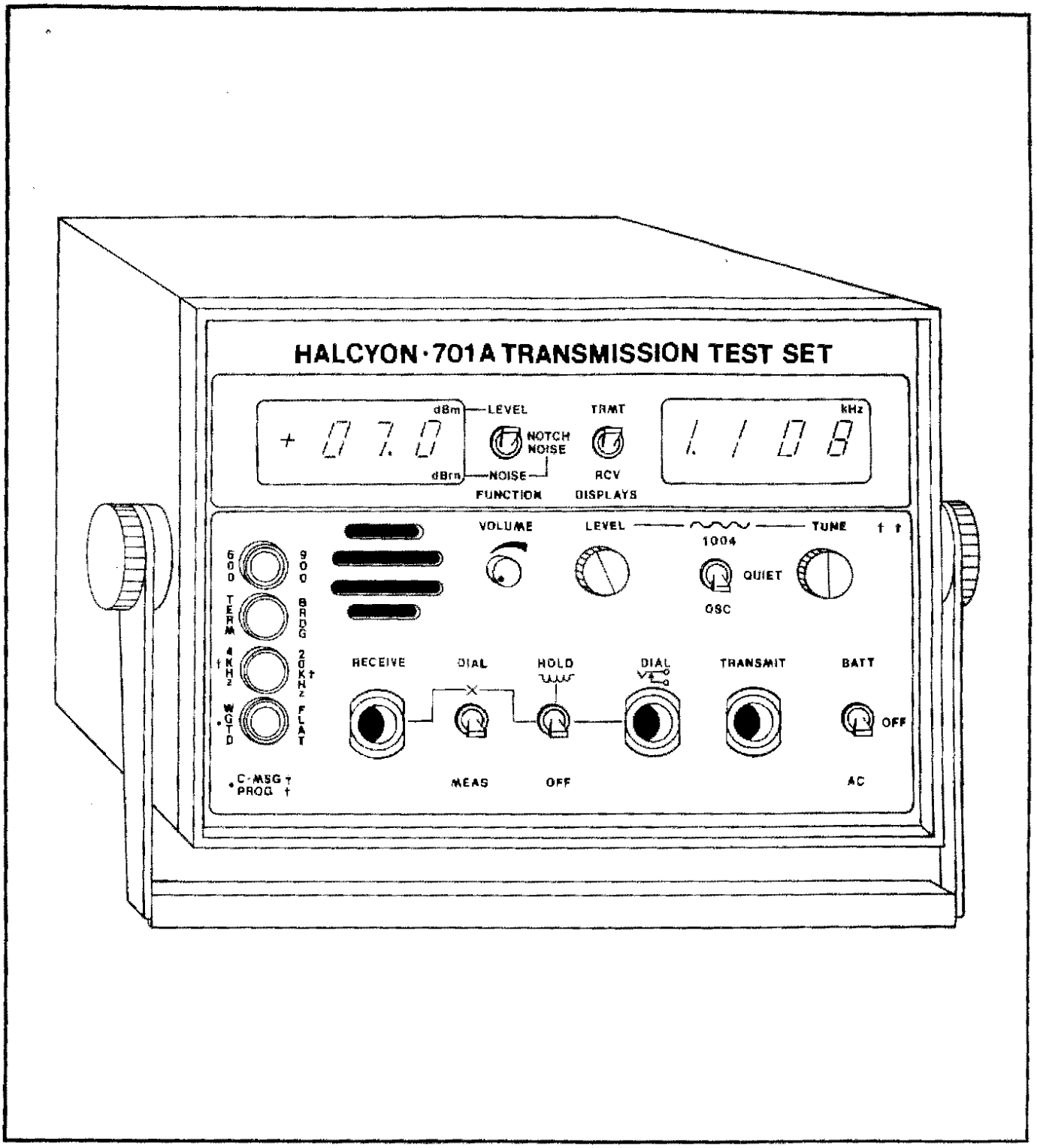

HALCYON·701A TRANSMISSION TEST SET
dBm
LEVEL
+ 07.0
dBrn
NOISE
FUNCTION
NOTCH
NOISE
TRMT
RCV
DISPLAYS
kHz
1.108
VOLUME
LEVEL
1004
TUNE
QUIET
OSC
600 TERM
900 BRDG
4KHz WGTD
20KHz FLAT
C-MSG PROG
RECEIVE
DIAL
MEAS
HOLD
OFF
DIAL
TRANSMIT
BATT
OFF
AC

Fig. 1

1. GENERAL INFORMATION

1.01 The Halcyon 701A and 702A are voice-band transmission test sets with level, noise, and frequency measurement capabilities in conformance with Bell Technical Reference PUB 41009. The 701A is compact, lightweight, and comes equipped with batteries (optional) to make the unit a completely portable test instrument. (See Figure 1.) The 702A is the rack-mount version of the 701A, requiring only 1-3/4 inches of mounting space. (See Figure 2.) The 702A normally operates from ac power, but may be equipped for operation from -48 Vdc office battery supplies. Special features include the following:

1.02 Dual Digital Displays. Different colored displays provide positive differentiation between Level/Noise (red) and Frequency (green) digital readouts.

1.03 Holding Tone Oscillator. A 1004-Hz holding tone is provided for use in measuring loss, noise with tone, transient impairments or other tests which require a tone having precise frequency control and spectral purity.

1.04 Voice Frequency Channel. For VF measurements, the transmitter bandwidth is from 50 Hz to 4 kHz. C-message and 3-kHz flat weighting networks are provided to measure noise on such circuits. A 1010-Hz notch filter can be used to notch out the 1004-Hz tone. This notched noise measurement mode is recommended for all transmission facilities with PCM or compandored carrier links.

1.05 Program Channel. For program channel measurements the transmitter bandwidth is from 4 kHz to 20 kHz. A program channel weighting network and a 15-kHz flat weighting network is provided to measure noise on such circuits. This feature is useful in checking local loops for conformance with digital data transmission or wideband program channel requirements.

1.06 Battery Charge Status Indications (701A only). Battery power supply circuits have been configured so that the 5-volt display and associated logic supply will discharge first, instead of the 9-volt supply that powers the basic measurement and signal-generation circuitry. Consequently, the display operation will give visual indication of a marginal battery charge. This visual indication will appear as a random but continuous flickering of either the Level/Noise or the Frequency display. When this occurs, battery operation should be discontinued and a recharge initiated before the unit is used again.

1.07 The 702A may be equipped for operation from a -48 Vdc office battery in facilities where this is the only source of power.

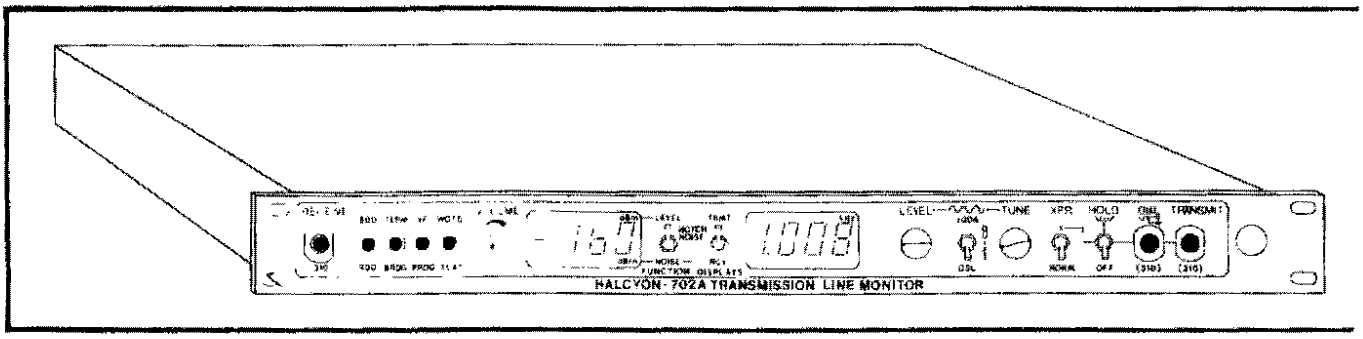


Fig. 2

2. PERFORMANCE SPECIFICATIONS

2.01 Transmitter:

- Holding Tone: 1004 Hz +/-0.1 Hz
- Oscillator Range: 50 Hz to 20 kHz (2 ranges)
- Output Level Range: -40 dBm to +13 dBm
- Tuning Control: Ten Turn Pot
- Level Control: Ten Turn Pot
- Distortion: <-50 dB, 200 Hz to 4 kHz
  <-40 dB, 50 Hz to 200 Hz and 4 kHz to 20 kHz

2.02 Receiver:

- Frequency Range: 50 Hz to 20 kHz
- Frequency Response: +/-0.1 dB, 200 Hz to 4 kHz
  +/-0.2 dB, 4 kHz to 15 kHz
  +/-0.5 dB, 50 Hz to 20 kHz
- Level Range: -50 dBm to +13 dBm
- Measurement Resolution: 0.1 dB
- Measurement Accuracy @ 1 kHz: +/-0.1 dB, -30 dBm to +13 dBm
  +/-0.2 dB, -30 dBm to -50 dBm

2.03 Frequency Counter:

- Frequency Range: 50 Hz to 20 kHz
- Level Range: -50 dBm to +13 dBm
- Measurement Resolution: 1 Hz, 50 Hz to 4 kHz
  10 Hz, 4 kHz to 20 kHz
- Measurement Accuracy: +/-1 Hz, 50 Hz to 4 kHz
  +/-10 Hz, 4 kHz to 20 kHz

2.04 Noise Measurement:

- Weighting Networks: C-Message, 3 kHz Flat Program, 15 kHz Flat
- Level Range: 10 dBrn to 99 dBrn
- Notch Attenuation: <-50 dB, 995 to 1025 Hz
- Measurement Resolution: 1 dB
- Measurement Accuracy: +/-1 dB

2.05 General:

- Input Impedance: 600 or 900 ohms 25K, Bridged
- Output Impedance: 600 or 900 ohms
- Power (701A): NiCd Batteries or 117/230 Vac 50/60 Hz
- Battery Capacity (701A): 5 hrs. Nominal
- Charger (701A): 117/230 Vac
- Charging Time (701A): 8 Hrs. Nominal
- Power (702A): -48 Vdc Office Battery or 117/230 Vac, 50/60 Hz
- Size (701A): 5" (12.7 cm) H x 7" (17.78 cm) W x 12" (30.48 cm) D
- Size (702A): 1 3/4" (4.44 cm) H x 19" (48.26 cm) W x 10" (25.4 cm) D
- Weight (701A): Approximately 10 lbs (4.5 kg)
- Weight (702A): 8 lbs. (3.6 kg)
- Environment: 0 to 50 deg. C
  0 to 90 percent Relative Humidity

3. THEORY OF OPERATION

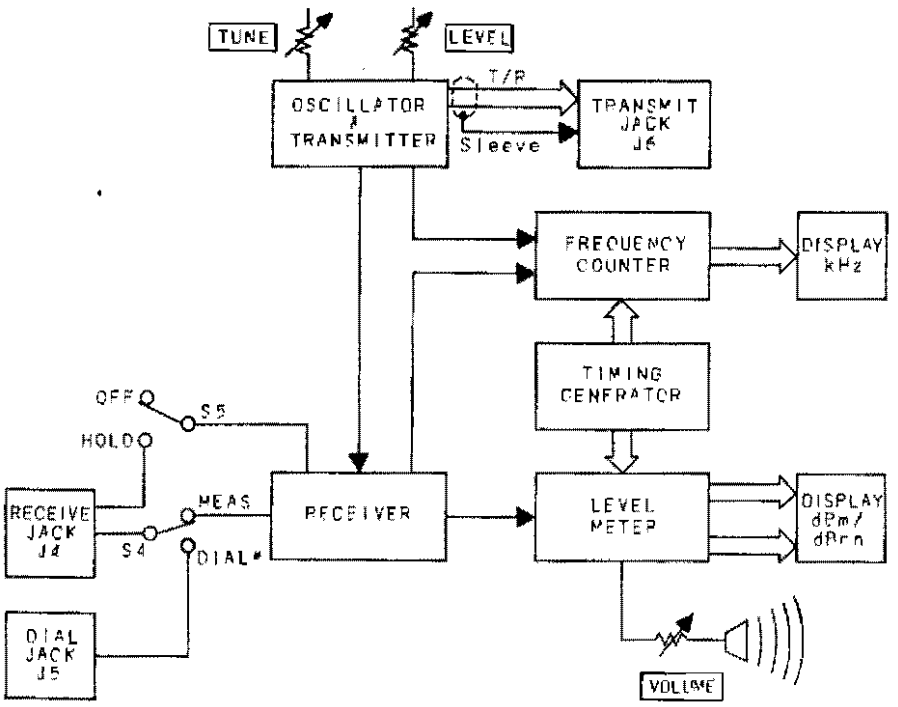
A. General

3.01 This section contains the theory of operation for the five major circuits of the 701A and 702A units. These are: (1) oscillator and transmitter, (2) receiver, (3) timing generator, (4) frequency counters and (5) level meter.

3.02 Block Diagrams: Figure 3 is a simplified functional block diagram of the 701A. The diagram is equally applicable to the 702A unit except as noted. Each of the sections depicted in Figure 3 is expanded by a detailed block diagram describing that particular section. The major sections shown are functional blocks and do not correspond to physical blocks in the actual unit. The physical locations of all major components are listed in the detailed block diagrams and can be correlated to the appropriate schematic diagram for detailed analysis of the circuit. For example, referring to Figure 4, assume you want to locate the VCO circuit on the schematic diagram. The block representing the VCO is labeled VCO and is further identified as IC11 and 1102; this means that the VCO circuit is an IC chip which is identified as IC11 and is located on schematic diagram SD-1102-00. (See Section 5.) The physical location of the chip is shown on the associated assembly drawing, ED-1102-00.

3.03 Schematic Diagrams: The schematic diagrams for the 701A and 702A units are located in Section 5 in numerical order. Three of the printed circuit boards (PCBs) used in the 701A unit are used also in the 702A unit. Hence, the schematics for these boards will not be duplicated and only one schematic diagram per board appears as reference for both units. The PCBs that are common to both units and share the same schematics are:

SD-1100-00	Level Meter PCB
SD-1101-00	Digital Level PCB
SD-2084-01	Termination PCB



*Refer to paragraph 3.21 for description of different dial and hold functions available.

Fig. 3

B. Oscillator and Transmitter (Figure 4)

3.04 VCO: The frequency of the VCO is controlled by the 4 kHz/20 kHz range switch and the TUNE control. The wiper of the TUNE control (R3) controls two current sources via buffer IC13. One current source controls the down ramp and the other current source controls the up ramp of the symmetrical triangular waveform output of the VCO (IC11). The 4 kHz/20 kHz range switch selects the different timing capacitors to the VCO - depending on the frequency range selected.

3.05 Sine Wave Shaping: The sine wave shaping circuit converts the VCO triangular waveform output into a sine wave via a diode network. The diodes are biased and conduct at programmed points of the input waveform to change the transfer function of the shaping circuit.

3.06 Oscillator Select: The 1004/QUIET/OSC switch controls the oscillator select, a dual analog switch. The selected oscillator signal is buffered by IC17, attenuated by the LEVEL control and buffered by IC20. The gain of IC20 is changed by the 600/900 termination switch to provide constant signal power across the termination. The gain is X1.22 for 900 ohms and X1 for 600 ohms.

3.07 Transmitter: The oscillator output signal from IC20 is fed via Quiet Select IC21, a dual analog switch, amplified by IC22, 23, and transformer coupled to the TRANSMIT Jack J6. The oscillator output can be disabled by the dual analog switch IC21 when the 1004/QUIET/OSC switch is placed in the QUIET position.

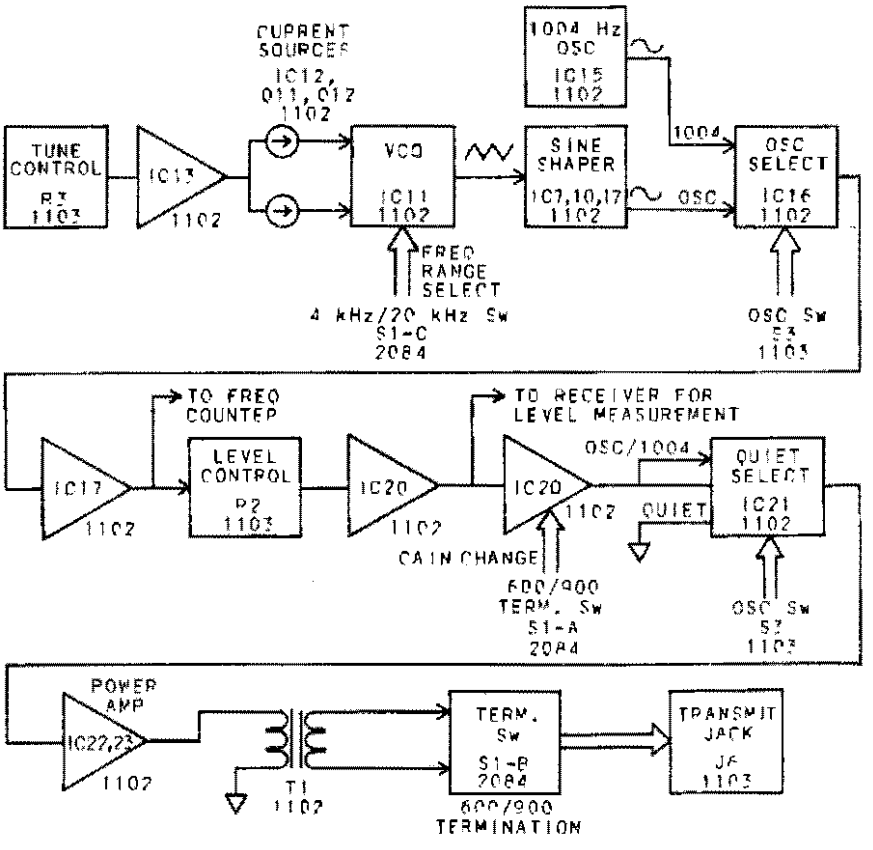


Fig. 4

C. Receiver (Figure 5)

3.08 Input Circuits: The hold circuit (Q4-Q6) is a constant-current source which is connected to the tip and ring contacts of the RECEIVE jack when the HOLD/OFF switch is placed in the HOLD position. The DIAL jack via its shorting contacts is connected to the RECEIVE jack when the DIAL/MEAS switch is placed in the DIAL position. The gain of IC10 is changed by the 600/900 termination switch to compensate for the power level change across the line termination. The 701A and 702A sample-and-hold circuits are further described in paragraphs 3.21 through 3.26.

3.09 Filter: The output from amplifier IC10 is fed to the following points: (1) directly to the frequency counter circuitry on the Common Analog PCB; (2) to Filter Select A, IC13 (a quad analog switch); (3) C-message filter; (4) program filter; and (5) 3 kHz filter. When IC13 is enabled by Filter Select Logic (IC17-19) the output from IC13 is buffered by IC9 and applied directly to Filter Select B (IC14) as a "receive level" signal, to the 15 kHz Filter, and the Notch Filter. When IC14 is enabled by the Filter Select Logic, one of its four inputs is switched to the level meter circuitry via IC12 and to the VOLUME control. The four selectable inputs are: (1) noise, (2) unfiltered receive level, (3) unfiltered transmit level, or (4) notch noise.

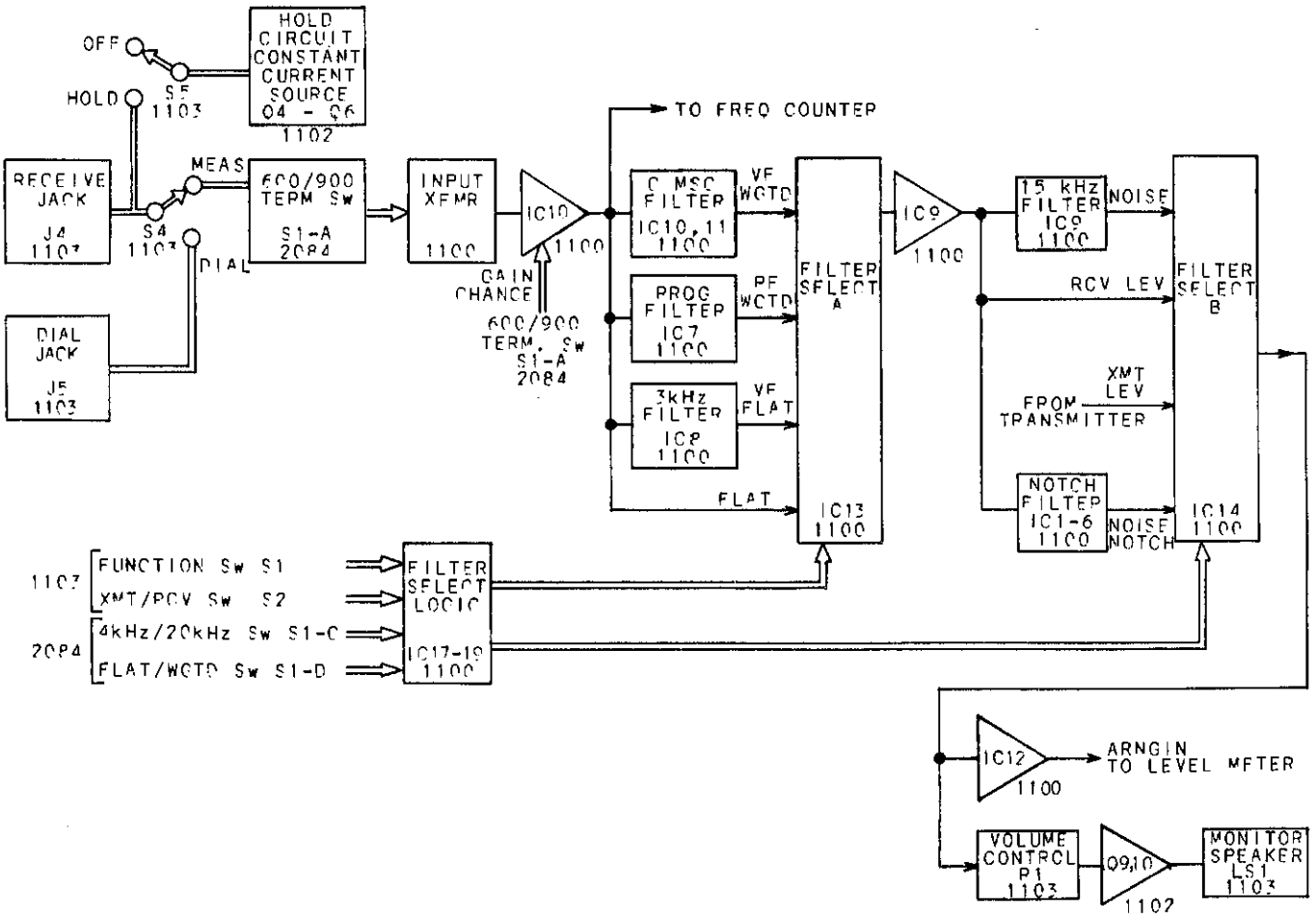


Fig. 5

D. Timing Generator (Figure 6)

3.10 Frequency Dividers: The 1-MHz oscillator signal is used by the Level Meter counting circuits. It is also divided by 1000 to obtain a 1-kHz signal (SCNFRQ) which is used by the Level Meter and Frequency Counter to multiplex the counter digits onto the decoder input lines. The 1-kHz signal is also divided by 10 to obtain a 100-Hz signal. This signal is in turn divided by 12 by two separate counters; one counts on the positive edges of the 100-Hz signal, and the other counts on the negative edges. Thus, the two counters are out of phase by one-half of the input period. The third stage of one counter provides a divide-by-6 output, which is further divided by 10 for use in the autoranging circuit in the Level Meter.

3.11 Timing Logic: Figure 7 shows the timing signals produced by combinations of the two divide-by-12 counters. Both counters count in binary until $\overline{C} \cdot \overline{D}$ resets both counters. The diagram shows the logic equation for each signal; these signals will be explained fully in the Frequency Counter and Level Meter descriptions.

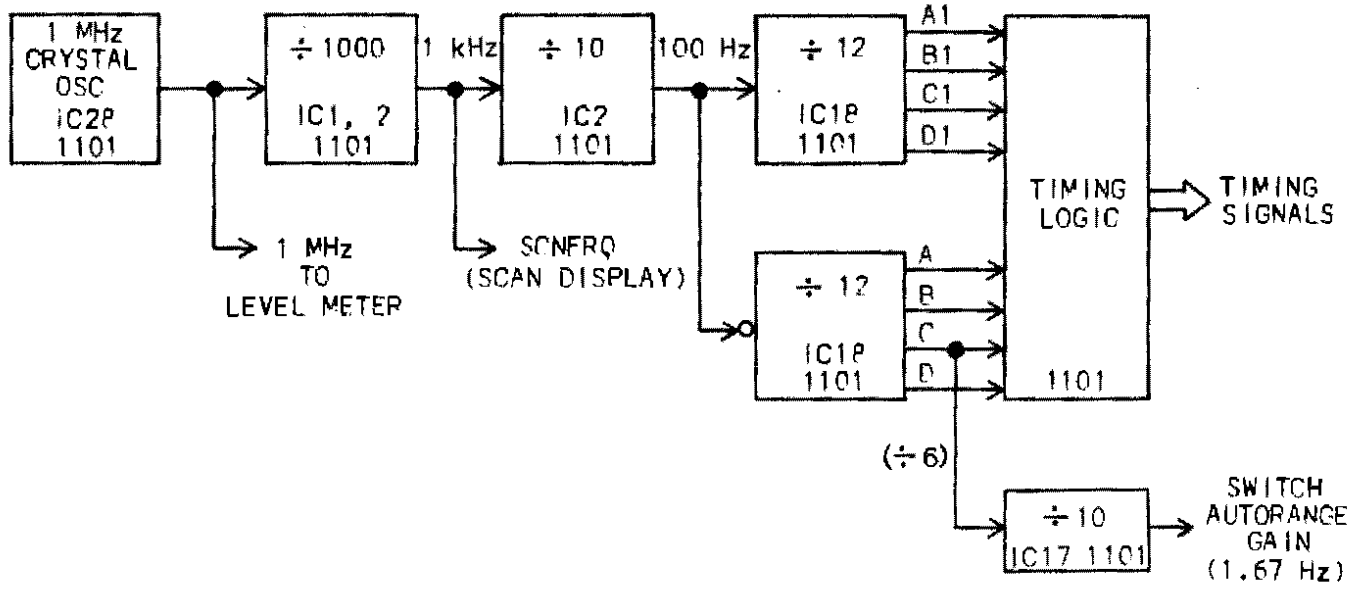


Fig. 6

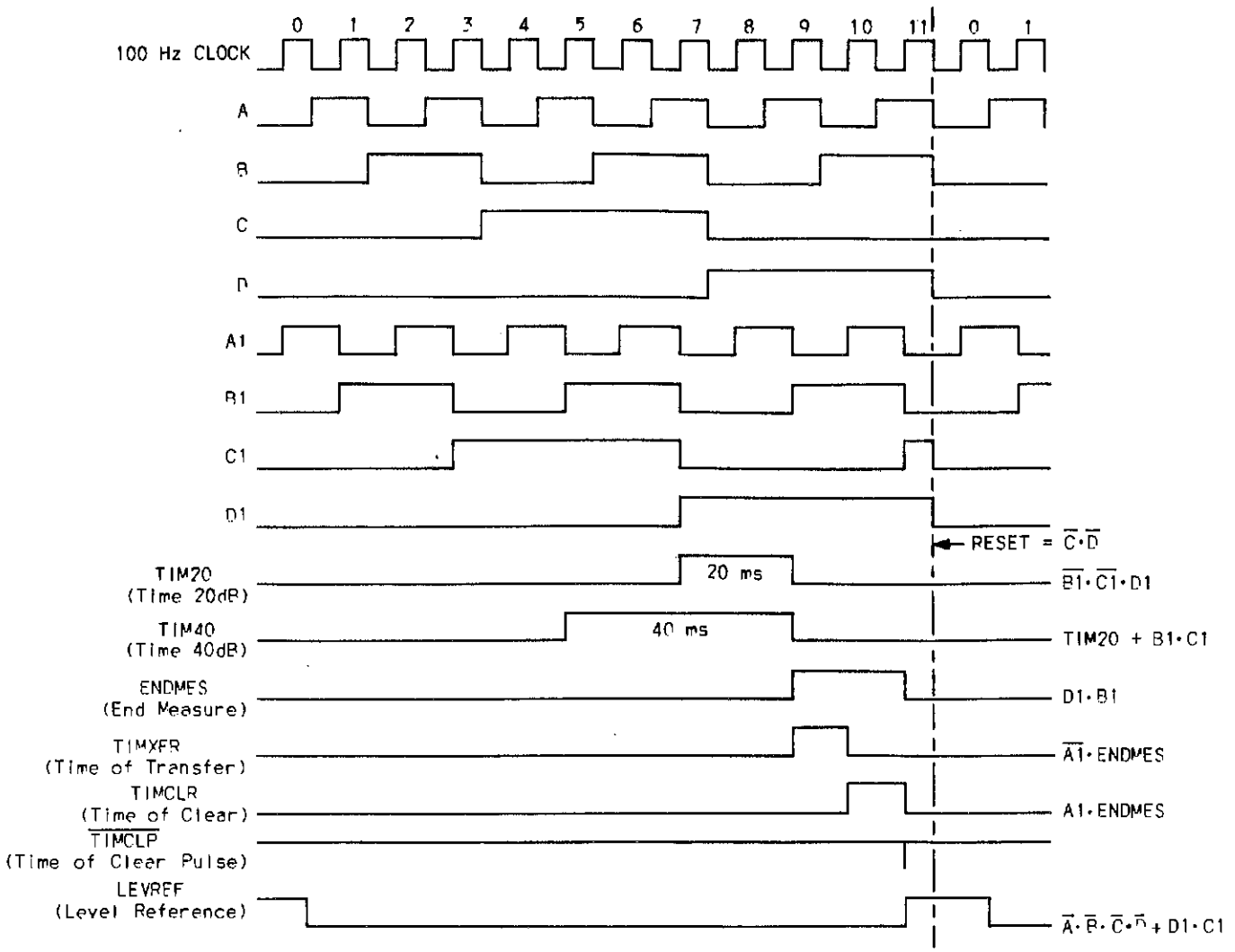


Fig. 7

E. Frequency Counter (Figure 8)

3.12 Input Circuits: The TRMT/RCV switch determines which input signal is selected. The low-pass filter removes noise spikes, and the square wave converter clips the signals to form a digital signal. The Frequency Select gating circuitry gates the square wave output or the output of a X10 frequency multiplier. The multiplier makes a 1 Hz resolution possible for a counter period of 0.1 second. The multiplier consists of a VCO, phase-locked loop and a divide-by-10 counter. The X10 signal is divided by 10 and compared with the input signal to correct the VCO frequency.

3.13 Counter and Display. The timing cycle begins with a $\overline{\text{TIMCLP}}$ signal (Time of Clear Pulse) which clears the 4-digit counter. The clear pulse is formed by differentiating the trailing edge of the TIMCLR signal (see Figure 7). The input signal is counted for 100 ms; the TIMXFR signal (Time of Transfer) overrides the input signal and transfers the counter contents to a storage register. The contents of the register are

continuously multiplexed onto the four bit data lines, one digit at a time. The multiplexing is controlled by the 1-kHz SCNFRQ (Scan Frequency) signal from the Timing Generator. The bit data is decoded by a BCD-to-seven segment decoder which controls the display segments through driver transistors.

3.14 Corresponding segments of all digits are wired together. The four-digit data lines indicate which digit is being multiplexed onto the bit data lines. Each digit data line feeds a driver which connects to the anode of all segments for a single digit. Therefore, any given segment of the display is lit by a coincidence of the segment driver and the digit driver. The display is blanked when the switches are set to QUIET and TRMT position. The decimal point is determined by the 4 kHz/ 20 kHz switch. The 4-Hz position gives X.XXX kHz; the 20-kHz position gives XX.XX kHz.

F. Level Meter (Figure 9)

3.15 Detectors: The input to the Level Meter is derived from Receiver Filter Select B (Figure 5), and consists of receiver noise, receiver level, receiver notch noise, or transmitter level. The signal is fed to an amplifier with a gain of 0, +20, or +40 dB. The gain is set by using the autoranging signal to switch, via a dual analog switch, feedback resistors in the amplifier. The output of the amplifier is fed to an Average Detector and a Peak Detector. The Average Detector output is selected for level measurements. The two detector outputs are summed to form a quasi-rms signal for noise measurements. The selected detector output, noise or level, is filtered to yield a dc output.

3.16 The dc output from the filter is compared with reference voltages that represent under-range, over-range, and out-of-range thresholds. The out-of-range comparator blanks the display; the under-range and over-range comparator outputs drive the Autorange Gain Switching logic. A two-bit counter stores the gain data (SD-1101-00):

AGC40 (40 dB gain) = Q1 (least significant bit)
AGC20 (20 dB gain) = Q2 (most significant bit)
$\overline{AGC}$ (0 dB gain) = $\overline{Q1} \cdot \overline{Q2}$

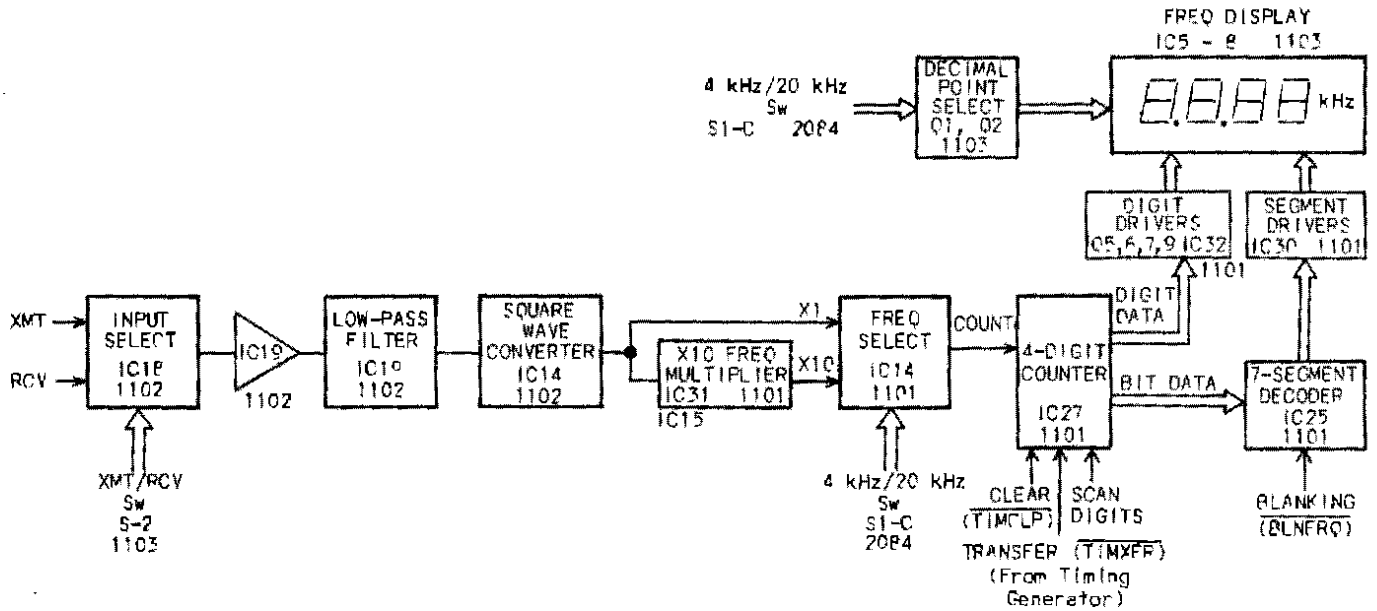


Fig. 8

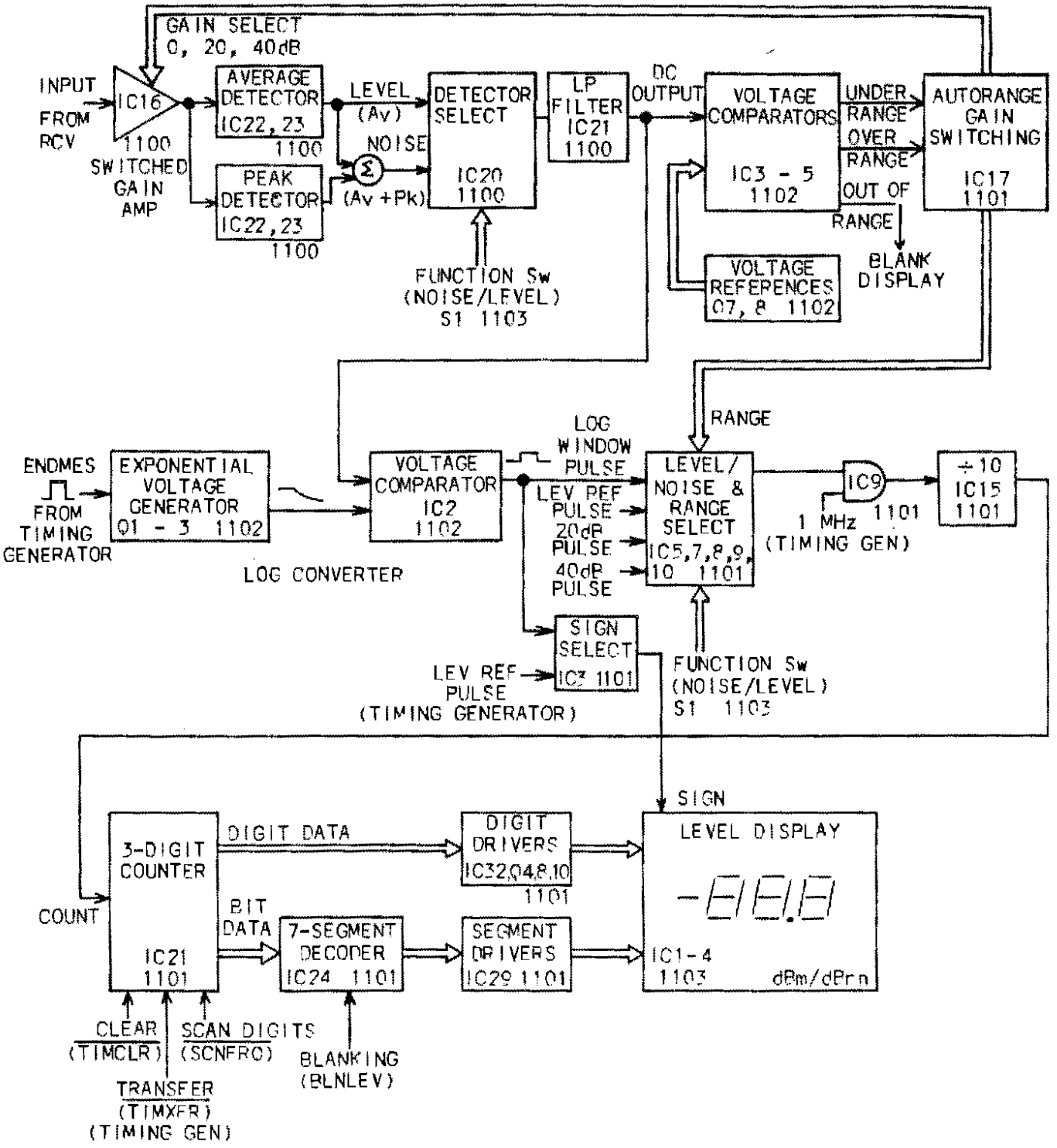

GAIN SELECT
0, 20, 40dB
INPUT
FROM
RCV
IC16
1100
SWITCHED
GAIN
AMP
AVERAGE
DETECTOR
IC22, 23
1100
PEAK
DETECTOR
IC22, 23
1100
LEVEL
(Av)
NOISE
(Av +Pk)
DETECTOR
SELECT
IC20
1100
LP
FILTER
IC21
1100
DC
OUTPUT
VOLTAGE
COMPARATORS
IC3 - 5
1102
UNDER
RANGE
OVER
RANGE
OUT OF
RANGE
AUTORANGE
GAIN
SWITCHING
IC17
1101
BLANK
DISPLAY
VOLTAGE
REFERENCES
Q7, 8 1102
FUNCTION Sw
(NOISE/LEVEL)
S1 1103
RANGE
ENDMES
FROM
TIMING
GENERATOR
EXPONENTIAL
VOLTAGE
GENERATOR
Q1 - 3 1102
LOG CONVERTER
VOLTAGE
COMPARATOR
IC2
1102
LOG
WINDOW
PULSE
LEV REF
PULSE
20dB
PULSE
40dB
PULSE
LEVEL/
NOISE &
RANGE
SELECT
IC5,7,8,9,
10 1101
IC9
1101
1 MHz
(TIMING GEN)
÷10
IC15
1101
SIGN
SELECT
IC? 1101
LEV REF
PULSE
(TIMING GENERATOR)
FUNCTION Sw
(NOISE/LEVEL)
S1 1103
SIGN
3-DIGIT
COUNTER
IC21
1101
COUNT
DIGIT DATA
DIGIT
DRIVERS
IC32,04,8,10
1101
LEVEL DISPLAY
-EE.E
IC1-4
1103
dBm/dPrn
BIT
DATA
7-SEGMENT
DECODER
IC24 1101
SEGMENT
DRIVERS
IC29 1101
CLEAR
(TIMCLR)
SCAN DIGITS
(SCNFRQ)
BLANKING
(BLNLEV)
TRANSFER
(TIMXFR)
(TIMING GEN)

Fig. 9

The counter steps for any of the following conditions:

Over-range • AGC40

+ (under-range + over-range) • AGC20

+ under-range • $\overline{AGC}$

3.17 A 1.67-Hz signal (CLK2HZ) from the Timing Generator is used as a counter clock. The counter resets whenever Q1•Q2 occurs; note that the counter steps from the AGC20 state for either over-range or under-range. The over-range condition steps the counter to the $\overline{AGC}$ state by resetting the counter. The under-range condition steps the counter once more to reach the AGC40 state. Figure 10 shows how the gain is switched for a decreasing signal and an increasing signal. Note the 2-dB hysteresis for the two cases. This avoids excessive gain switching for signals which fluctuate at the gain boundaries. The hysteresis is provided by the voltage comparators. The under-range comparator turns on for input voltages less than 0.074 volts, while the over-range comparator turns on for inputs greater than 1.11 volts. The autoranging gain signals are fed back to the input amplifier to set the gain, and are also fed to the Level Meter Logic to correct the display.

3.18 Log Converter: Figure 11 shows the operation of the log converter. The ENDMES (End Measure) pulse from the Timing Generator charges a capacitor to a reference voltage. At the end of the pulse, the capacitor is allowed to discharge through a resistor. The capacitor voltage is buffered by a high impedance amplifier and compared with the dc voltage that represents the input signal level. The output of the comparator is high from the start of the ENDMES pulse until the capacitor voltage is less than the input voltage. The width of the comparator output is inversely proportional to the log of the input voltage.

3.19 Counter Logic: The output pulse of the log converter comparator (LOGWND) is used as a "window" to gate 1 MHz clock pulses to the 3-digit counter which drives the level display. Addi-

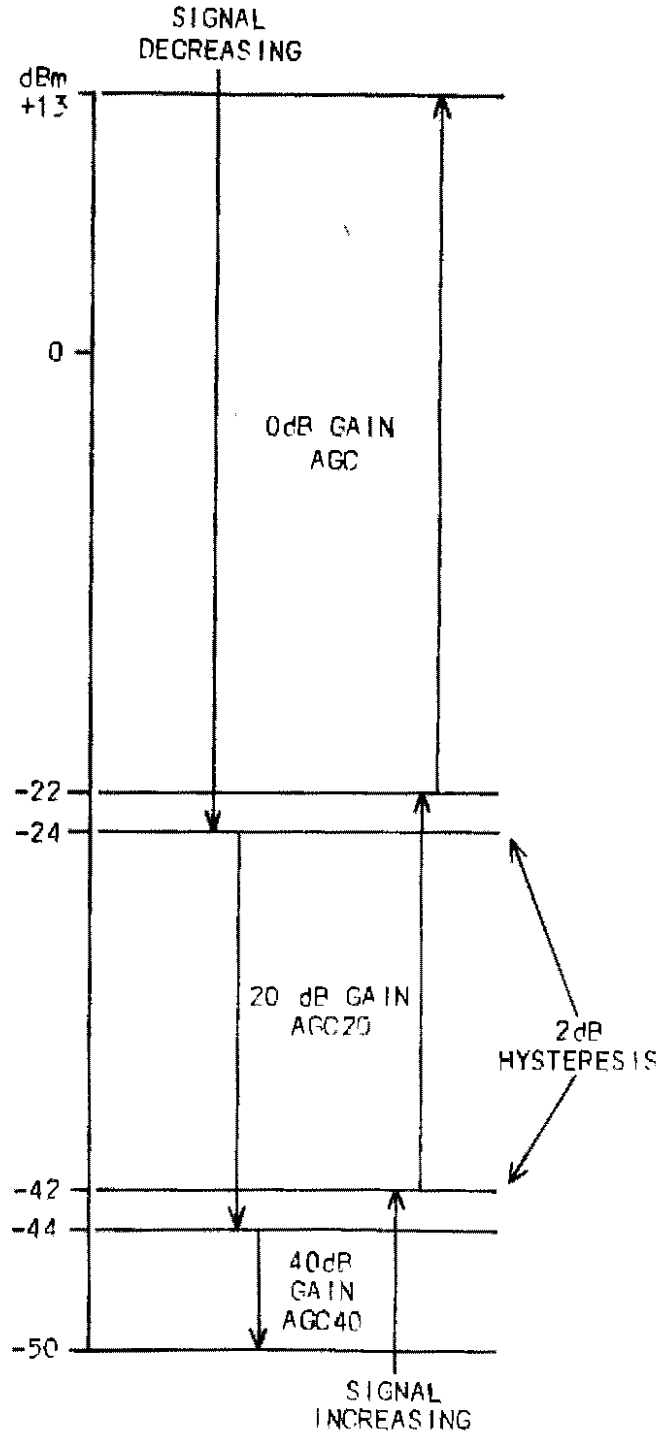


Fig. 10

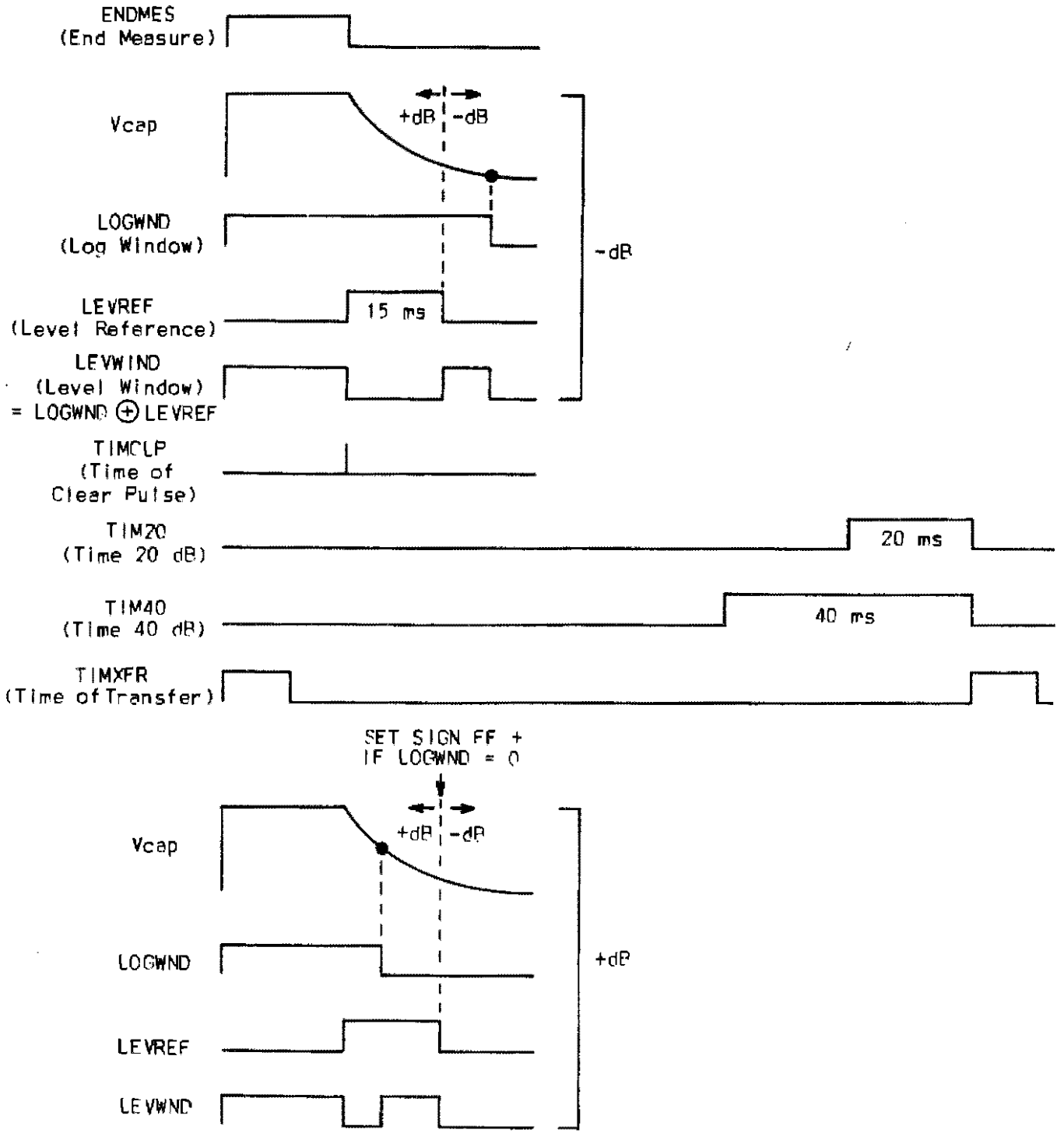

ENDMES
(End Measure)
Vcap
+dB
-dB
LOGWND
(Log Window)
-dB
LEVREF
(Level Reference)
15 ms
LEVWIND
(Level Window)
= LOGWND ⊕ LEVREF
TIMCLP
(Time of
Clear Pulse)
TIM20
(Time 20 dB)
20 ms
TIM40
(Time 40 dB)
40 ms
TIMXFR
(Time of Transfer)
SET SIGN FF +
IF LOGWND = 0
Vcap
+dB
-dB
LOGWND
+dB
LEVREF
LEVWND

Fig. 11

tional window pulses are added to correct the display for the selected gain.

(a) Negative dB Level Measurements: Figure 11 shows the timing for level measurements. The first case shown is a negative dB level. A LEVWIND (level window) signal is formed when:

$$LEVWND = LOGWND \oplus LEVREF$$

LEVREF (level reference) is a 15 ms pulse from the timing generator. The timing cycle begins with the clearing of the counter with TIMCLP. The counter input for level measurements is:

$$1\ MHz \cdot TIMXFR \cdot (LEVWND + AGC20 \cdot TIM20 + AGC40 \cdot TIM40)$$

Only the portion of LOGWND that follows the end of LEVREF is counted. The portion during LEVREF is blocked by the exclusive OR; the portion before LEVREF is cleared by TIMCLP. Note that the count increases as the input level decreases. The count pulses are divided by 10 and fed to the 3-digit counter. (The counter is actually a 4-digit counter; the LSD is not displayed. Therefore, an additional division by 10 is inserted.)

(b) Scaling: Proper scaling of the display is provided by the TIM20 and TIM40 pulses. The 20 ms TIM20 pulse is gated by AGC20 to add 20,000 pulses to the count. Dividing these pulses by 10^4 results in a display of 200. Since the display is in tenths of dB, 20.0 dB is added. TIM40 is used in a similar manner for the 40 dB range, and neither signal is used for the 0 dB range. The contents of the counter are transferred to a storage register at the TIMXFR pulse (Time of Transfer). Counting is blocked during this pulse.

(c) Positive dB Level Measurements: The second case shown in Figure 11 is a positive level measurement. The counter is enabled from the end of LOGWND until the end of LEVREF. Note that the count decreases as the input level decreases. The sign of the display is determined by a FF, which is set high (positive signal) if LOGWND is low at the end of LEVREF. The displayed + sign is formed by a combination of the - sign and a vertical line.

(d) Noise Measurements: Noise measurements are displayed in reverse notation, i.e., dBrn. 0 dBm corresponds to 90 dBrn and -90 dBm corresponds to 0 dBrn. Figure 12 shows the log conversion. A NOIWND (noise window) signal is formed when:

$$NOIWND = (\overline{TIM40} \cdot \overline{LOGWND}) + TIMCLR$$

The timing cycle begins with the clearing of the counter with TIMCLP. The counter input for noise measurements is:

$$1\ MHz \cdot \overline{TIMXFR} \cdot (NOIWND + TIM20 \cdot AGC20 + TIM40 \cdot \overline{AGC20} \cdot \overline{AGC40})$$

Figure 12 shows that NOIWND enables the counter from the end of LOGWND to the beginning of TIM40. Note that the count decreases as the noise level decreases. Proper scaling is provided by adding the TIM20 pulse for the 20 dB range, TIM40 for the 0 dB range, or neither for the 40 dB range. TIMXFR blocks the counting at the end of the cycle and transfers the counter contents to the storage register. The counter requires at least one additional count pulse to transfer the counter contents. This requirement is met by the TIMCLR term in the equation for NOIWND.

3.20 Level Display: The operation of the level display is similar to that of the Frequency Meter Display (paragraph 3.13). The sign, decimal point, and tenths digit are blanked for noise measurements. The level display

is blanked with the plus sign on whenever a level measurement exceeds +13 dBm. Conversely, the display is blanked with the minus sign on whenever the controls are set to TRMT and QUIET position. The entire display is blanked when the controls are set to TRMT and NOISE or NOTCH NOISE.

G. Logic Equations

$$ENDMES = D1 \cdot B1$$
(End Measure)

$$TIM20 = C1 \cdot (\overline{\overline{D1} + B1}) = \overline{C1} \cdot D1 \cdot \overline{B1}$$
(Time 20 dB)

$$TIM40 = B1 \cdot \overline{C1} + TIM20 = B1 \cdot C1 + \overline{C1} \cdot D1 \cdot \overline{B1}$$
(Time 40 dB)

$$TIMXFR = \overline{A1} \cdot ENDMES = \overline{A1} \cdot B1 \cdot D1$$
(Time of Transfer)

$$TIMCLR = A1 \cdot ENDMES = A1 \cdot B1 \cdot D1$$
(Time of Clear)

$$LEVREF1 = C + D + A + B$$

$$LEVREF = LEVREF1 + (D1 \cdot C1)$$
(Level Reference)

$$LEVWND = LOGWND \cdot \overline{LEVREF} + \overline{LOGWND} \cdot LEVREF = LOGWND \oplus LEVREF$$
(Level Window)

$$NOIWND = TIMCLR + (\overline{TIM40} \cdot \overline{LOGWND})$$
(Noise Window)

$$COUNT = 1MHZ \cdot \overline{TIMXFR} \cdot [(\overline{LEVEL} \cdot (TIM20 \cdot AGC20 + TIM40 \cdot \overline{AGC20} \cdot \overline{AGC40} + NOIWND)]$$

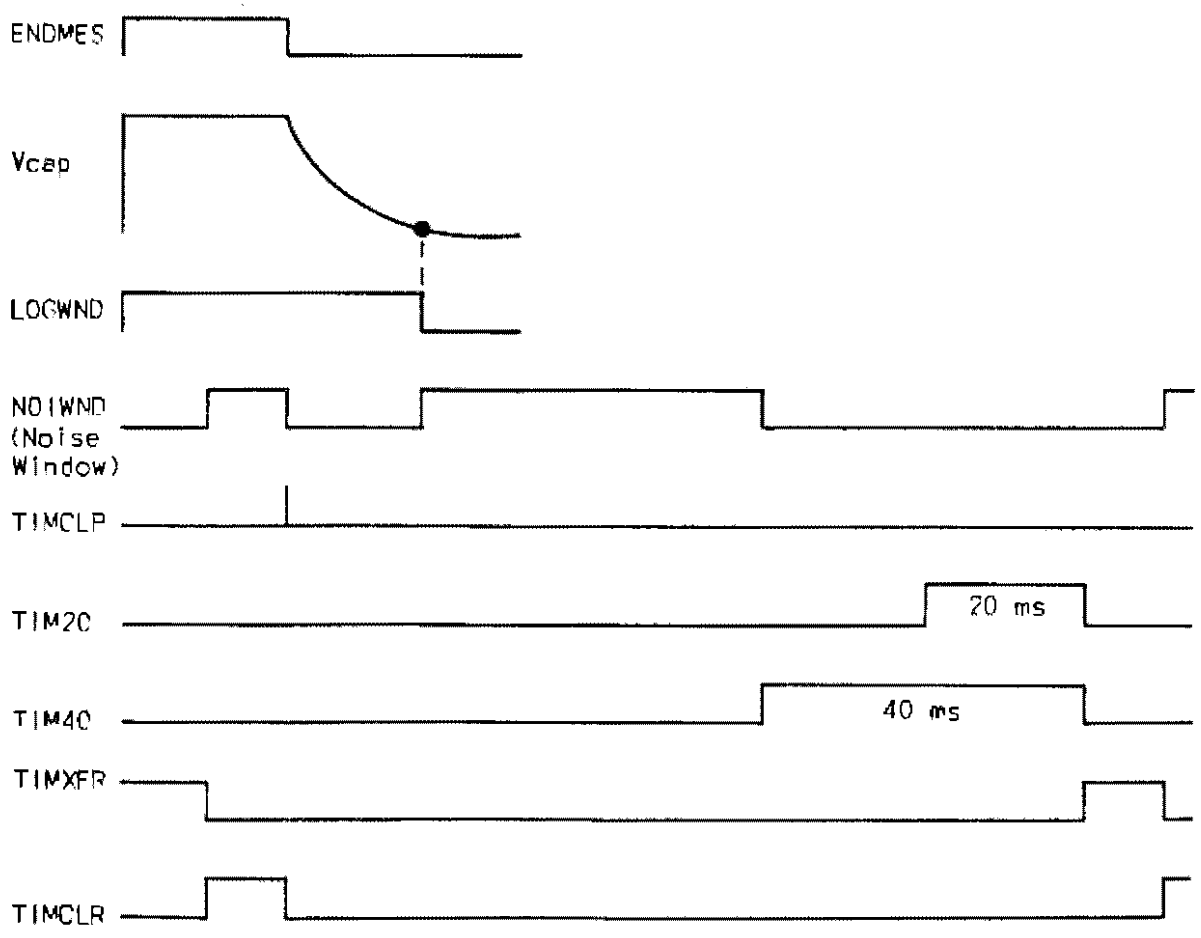


Fig. 12

+ LEVEL · (AGC40 · TIM40 + AGC20 · TIM20 + LEVWND)

NEGSGN = BLNFRQ + LEVEL
(Negative Sign)

POSSGN = LEVEL · FF3 (+ sign formed by POSSGN · NEGSGN)
(Positive Sign)

$FF3_J = \overline{LOGWND}$ [(FF3 (IC3-1, 1101) is 1 for +, 0 for -)]

$FF3_K = LOGWND$

$FF3_{CLK} = \overline{LEVREF}$

BLNFRQ = QUIET · XMT
(Blank Frequency)

BLNLEV = OUTRNG + QUIET · XMT + $\overline{LEVEL}$ · XMT
(Blank Level)

$\overline{FRQCNT}$ = VF · INPUT X10 + $\overline{VF}$ · INPUT + TIMXFR
(Frequency Count)

AGC20 = Q2 (IC17-12, 1101)
(Auto Gain Control 20)

AGC40 = Q1 (IC17-11, 1101)

$\overline{AGC} = \overline{Q1} \cdot Q2$

Switch AGC = CLK2HZ · [UNDRNG · $\overline{AGC20}$ · $\overline{AGC40}$ + (UNDRNG + OVRRNG) · AGC20 + OVRRNG · AGC40)]

UNDRNG - Under-range
OVRRNG - Over-range

Reset AGC = Q1 · Q2

VF = 4kHz switch position

PROG = 20kHz switch position

LEVREC = LEVEL · REC

LEVXMT = LEVEL · XMT

FLAT = LEVEL + $\overline{(WGTD + VF)}$

$VFWGTD = \overline{LEVEL} \cdot VF \cdot WGTD$
(C Message Filter)

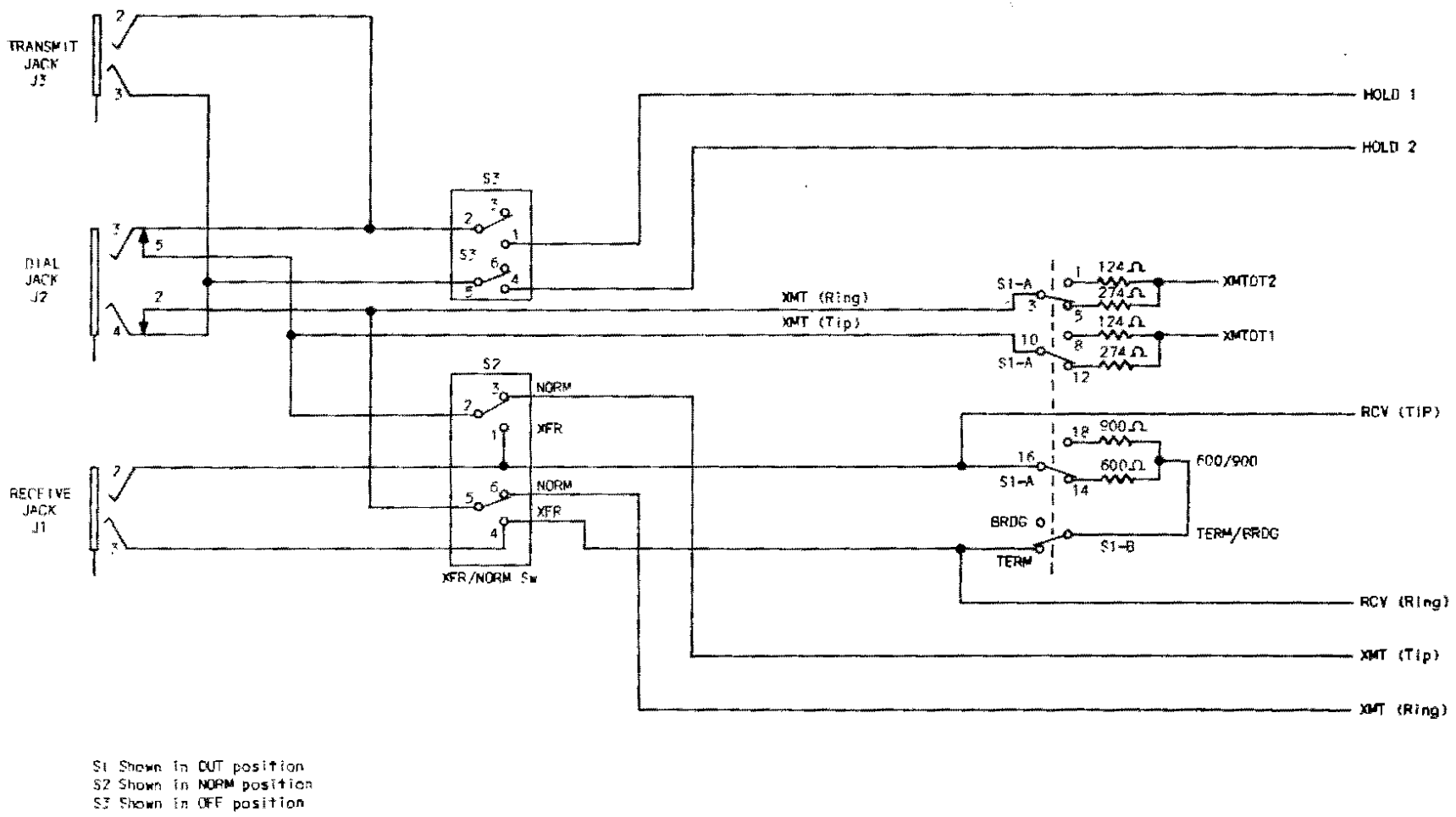
PFWGTD = LEVEL PROG WGTD
(Program Filter)

$VFFLAT = \overline{LEVEL} \cdot \overline{PROG} \cdot \overline{WGTD}$
(3 kHz Filter)

H. Dial and Hold Functions

3.21 Variations of the Dial and Hold function have been incorporated in the 701A units manufactured to date. The functional differences and effective serial numbers are described in the following paragraphs.

3.22 701A Units, S/N up thru 1502: Units with serial numbers up thru 1502 have the dial and hold function associated with the TRANSMIT (output) jack. (See Figure 13.) When a dial set is plugged into the DIAL jack, both the receive and transmit internal measurement circuits are disconnected from the TRANSMIT jack, and a direct connection is established between the DIAL jack and the TRANSMIT jack. This arrangement permits the circuit under test to be connected to the TRANSMIT jack, and to be dialed up using a dial set plugged into the DIAL jack. When an off-hook condition is established at the far-end, and with the HOLD/OFF switch in the HOLD position, a holding current is applied to the line under test. Removal of the dial set from the DIAL jack establishes a connection from the TRANSMIT jack to the internal measurement circuitry which is controlled by the XFR/NORM switch. With the switch in the XFR position, the measurement circuitry is connected to the circuit under test and the transmit circuitry is disconnected. In the NORM position, the transmit measurement circuitry is connected to the circuit under test to allow application of the oscillator output. The units having this particular arrangement can be identified by the presence of the XFR/NORM toggle switch on the front panel.

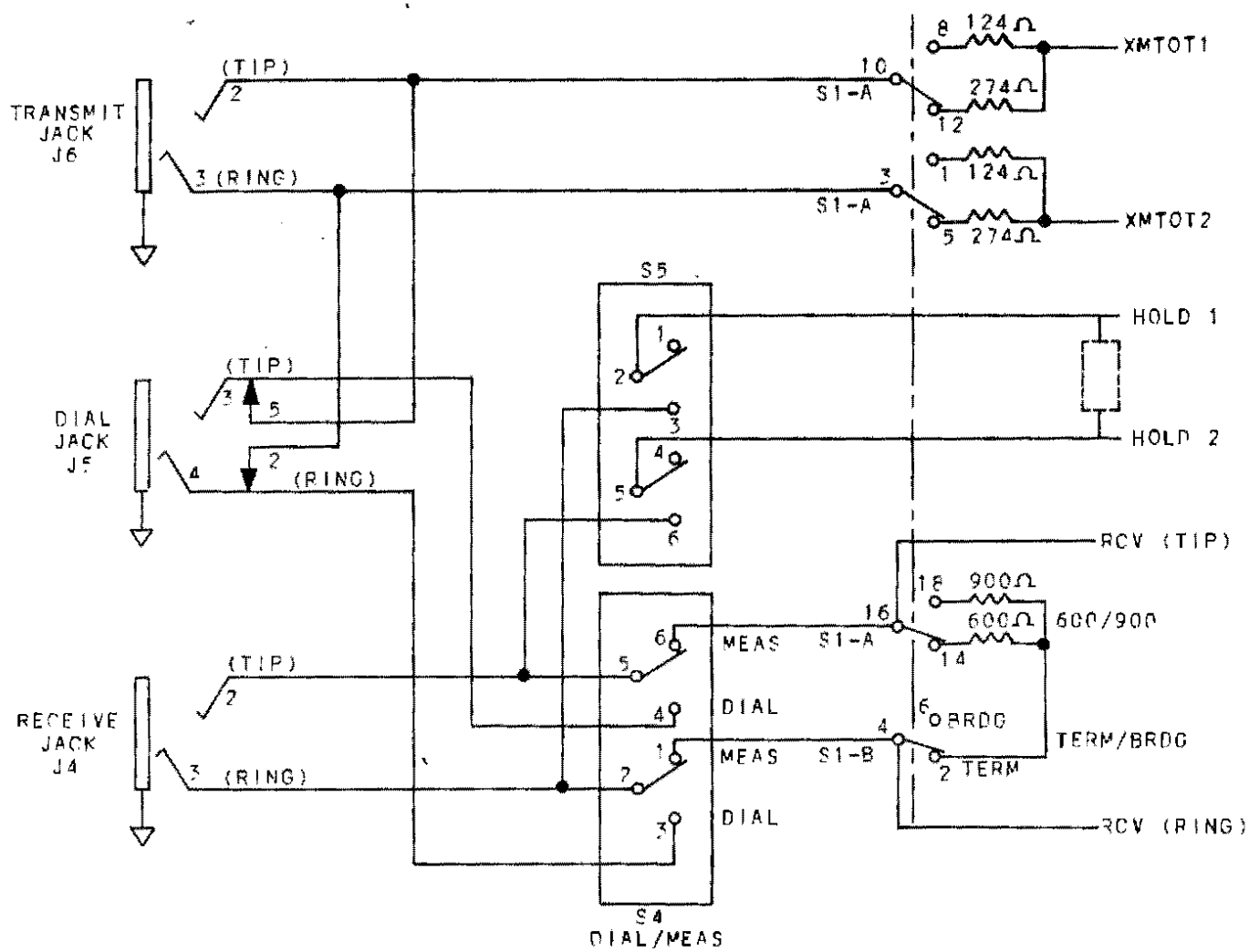


S1 Shown in OUT position
S2 Shown in NORM position
S3 Shown in OFF position

Fig. 13

3.23 701A Units, S/N 1656 including all subsequent serial numbers except 1662 thru 1668: The current production units incorporate a DIAL/MEAS switch (in lieu of the XFR/NORMAL switch), and have the dial/hold function assigned to the RECEIVE jack. (See Figure 14.) With the circuit under test patched to the RECEIVE jack and a dial set plugged into the DIAL jack, the circuit under test can be dialed up when the DIAL/MEAS switch is placed in the DIAL position. Upon establishing an off-hook condition at the far-end, and placing the DIAL/MEAS switch in the MEAS position, the internal receive measurement circuitry is connected to the circuit under test. If only a measurement test is required, it is not necessary to remove the dial set from the DIAL jack.

3.24 Most circuits will be held up by the 600 or 900 ohm resistive termination across Tip and Ring. However, for extended loops, additional holding current can be provided by placing the HOLD/OFF switch in the HOLD position. If it is desired to apply a test tone signal, the HOLD/OFF switch must be



S1 Shown in OUT position

S4 Shown in MEAS position

S5 Shown in OFF position

Fig. 14

placed in the HOLD position, the dial set must be removed from the DIAL jack (if one is connected), and the DIAL/MEAS switch must be returned to the DIAL position. With a dial set removed, the DIAL/MEAS switch functions as a transmit measure switch connecting the circuit under test to the transmit circuit or the measurement circuitry respectively.

3.25 701A Units, S/N 1503 thru 1655 and 1662 thru 1668: A relatively small number of units were manufactured similar to the current version (refer to Paragraph 3.23 and 3.24), but without the capability to connect the transmit output to the dialed up circuit. The front panel arrangement of these units is the same as the current production version.

3.26 702A DIAL and HOLD Function (Figure 13): The 702A units have the same dial and hold configuration as the early 701A models (paragraph 3.22).

4. TEST AND CALIBRATION

A. 701A and 702A Test and Calibration Procedures

4.01 The following procedure is applicable to both the 701A and 702A test sets.

4.02 Test Equipment Required: The following test equipment is required for calibrating the 701A and 702A test sets.

- Multimeter
- RMS Voltmeter
- Distortion Analyzer
- Frequency Counter
- Oscillator
- Oscilloscope
- Attenuator
- Dc Power Supply

4.03 Initial Set-Up Procedure: Set the front panel switches on the 701A or 702A as follows:

FUNCTION switch	LEVEL
DISPLAYS switch	RCV
All pushbutton switches	Out (disengaged)

4.04 Jack Connections Test: Check the front panel jacks as follows:

(a) Check and verify that the Tip and Ring of the RECEIVE, TRANSMIT, and DIAL jacks are not connected to ground.

(b) Check and verify that the sleeves of all three jacks are connected to analog ground.

(c) Turn on power to the unit being tested.

4.05 Level Calibration Test: Perform the level calibration test as follows:

(a) Input a 0.0 dBm signal at 1 kHz and verify that it reads 0.0 dBm on an RMS meter (600 ohms termination).

(b) Adjust R10 (8000-1100-00) for a reading of +/-0.0 on the level display.

(c) Put 20 dB attenuation in the input signal.

(d) Adjust R1 (8000-1102-00) for a reading of -20.0 dBm on the level display.

(e) Put 40 dB attenuation in the input signal.

(f) Adjust R8 (8000-1100-00) for a reading of -40.0 dBm on the level display.

(8000-1102-00)
R1 IS NOT THE 1ST POT
IT IS 5TH FROM THE RIGHT VIEWED FROM THE REAR

(g) Repeat step (a) until the following conditions are met.

RMS Meter	Level Display
+13.0 dBm	+13.0 +/-0.2 dBm
0.0 dBm	0.0 +/-0.1 dBm
-10.0 dBm	-10.0 +/-0.2 dBm
-20.0 dBm	-20.0 +/-0.2 dBm
-30.0 dBm	-30.0 +/-0.2 dBm
-40.0 dBm	-40.0 +/-0.2 dBm
-50.0 dBm	-50.0 +/-0.2 dBm

4.06 Noise Calibration Test: Perform the noise calibration test as follows:

(a) Set FUNCTION switch to NOISE position.

(b) Input a 0.0 dBm, 1000 Hz signal.

(c) Adjust R9 (8000-1100-00) for a reading of 90 dBrn on the level display.

(d) Put 40 dB attenuation in the input signal.

(e) Adjust R7 (8000-1100-00) for a reading of 50 dBrn on the level display.

(f) Repeat step (b) until the following conditions are met.

RMS Meter	Level Display
0.0 dBm	90 +/-1 dBrn
-10.0 dBm	80 +/-1 dBrn
-20.0 dBm	70 +/-1 dBrn
-30.0 dBm	60 +/-1 dBrn
-40.0 dBm	50 +/-1 dBrn
-50.0 dBm	40 +/-1 dBrn

4.07 Transmitter Level Calibration Test: Perform the transmitter level calibration test as follows:

(a) Set DISPLAYS switch to TRMT position and select ~~1004 Hz~~ OSC mode 1000 Hz mode.

(b) Adjust front panel LEVEL control for a level display reading of 0.0 dB.

(c) Adjust R9 (8000-1102-00) until RMS meter (600 ohms terminated) reads 0.0 +/-0.1 dBm.

4.08 Transmitter Frequency Calibration Test: Perform the transmitter frequency calibration test as follows:

(a) Set DISPLAYS switch to TRMT mode and select OSC mode at 0.0 dB, 300 Hz.

(b) Adjust ~~R5~~ R2, R3, R7, R5 ~~R6~~, ~~R7~~ (8000-1102-00) for distortion of -50 dB.
NOTE R7 CHANGES FREQ - CHASE IT WITH DIST ANAL.

(c) Change transmitter frequency to 50 Hz.

(d) Adjust R4 (8000-1102-00) for distortion of -40 dB.

(e) Change transmitter frequency to 3000 Hz.

(f) Adjust R7 (8000-1102-00) for distortion of -48 dB. NOTE

(g) Repeat steps (a) thru (f) until the distortion specifications are satisfied.

4.09 1004 Hz Test: Perform the 1004 Hz test as follows:

(a) Set DISPLAYS switch to TRMT position, and select 1004 Hz mode.

(b) Adjust R8 (8000-1102-00) for a frequency display of 1005 Hz.
(c) ADJ R127 FOR 0.0 DBm OUTPUT

B. ED-1101-00 (Digital Level PCB) Test Procedure

4.10 The following test procedure is applicable to both the 701A and 702A test sets:

4.11 Test Equipment Required: The following test equipment is required for performing this test procedure:

701A or 702A (calibrated)
Frequency Counter
Halcyon 520B
Attenuator

4.12 Initial Set-Up Procedure: Set the front panel switches on the 701A or 702A unit as follows:

FUNCTION switch	LEVEL
DISPLAYS switch	RCV
All pushbutton switches	Out (disengaged)

4.13 Displays Test: Perform the displays test as follows:

(a) Input a 1000 Hz signal at 0.0 +/- 0.1 dBm into the RECEIVE Jack.

(b) The level display should read 0.0 dBm +/- 0.1 dBm and the frequency display should read 1.000 kHz.

(c) Observe that the frequency display does not change more than 1 Hz in least significant digit at a rate not less than one minute.

(d) The level display should not change or flicker.

(e) Both displays should be of equal brightness and readable.

4.14 Autoranging Test: Perform the autoranging test as follows:

(a) Change input level to -20.0 +/-0.1 dBm.

(b) The level display should change to -20.0 +/-0.1 dBm within 2 seconds and stay at that point.

(c) Change input level to -40.0 +/-0.1 dBm.

(d) The level display should change to -40.0 +/-0.2 dBm within 2 seconds and stay at that point.

4.15 Noise Test: Perform the noise test as follows:

(a) Set FUNCTION switch to NOISE position.

(b) Input the following signals and observe the level display.

Input Signal	Level Display Reading
0.0 +/-0.1 dBm	90 +/-1 dBrn
-20.0 +/-0.1 dBm	70 +/-1 dBrn
-40.0 +/-0.1 dBm	50 +/-1 dBrn
-60.0 +/-0.1 dBm	30 +/-1 dBrn

4.16 Frequency Resolution Test: Resolution should be 1 Hz for the 4 kHz range and 10 Hz for the 20 kHz range.

4.17 Blanking Logic Test: Perform the blanking logic test as follows:

(a) Set DISPLAYS switch to TRMT position.

(b) Set FUNCTION switch to NOISE position.

(c) Observe that the level display is blanked.

(d) Set the 1004/QUIET/OSC switch to QUIET position.

(e) Observe that both displays blank out except for the +/- sign and the decimal point.

(f) Input a signal 13.5 +/-0.4 dBm. The level display should be blanked except for the +/- sign and the decimal point.

(g) Except for the above conditions or low battery, the displays should not blank out in any other modes.

(h) Turn off power to the unit under test.

(i) This completes the test procedure for the Digital Level PCB (ED-1101-00).

5. ENGINEERING DRAWINGS

5.01 This section contains the Halcyon engineering drawings required for maintenance of the 701A and 702A test sets. The block and final assembly draawings are included first to aid in identifying the subassembly drawings that follow. The subassembly drawings are in numerical order as indicated by the four-digit base number and the two-digit suffix. All the drawings required for each assembly or subassembly are grouped together, with the schematic diagram followed by the assembly drawing, bills of material, and wiring list as applicable. The drawings included are as follows:

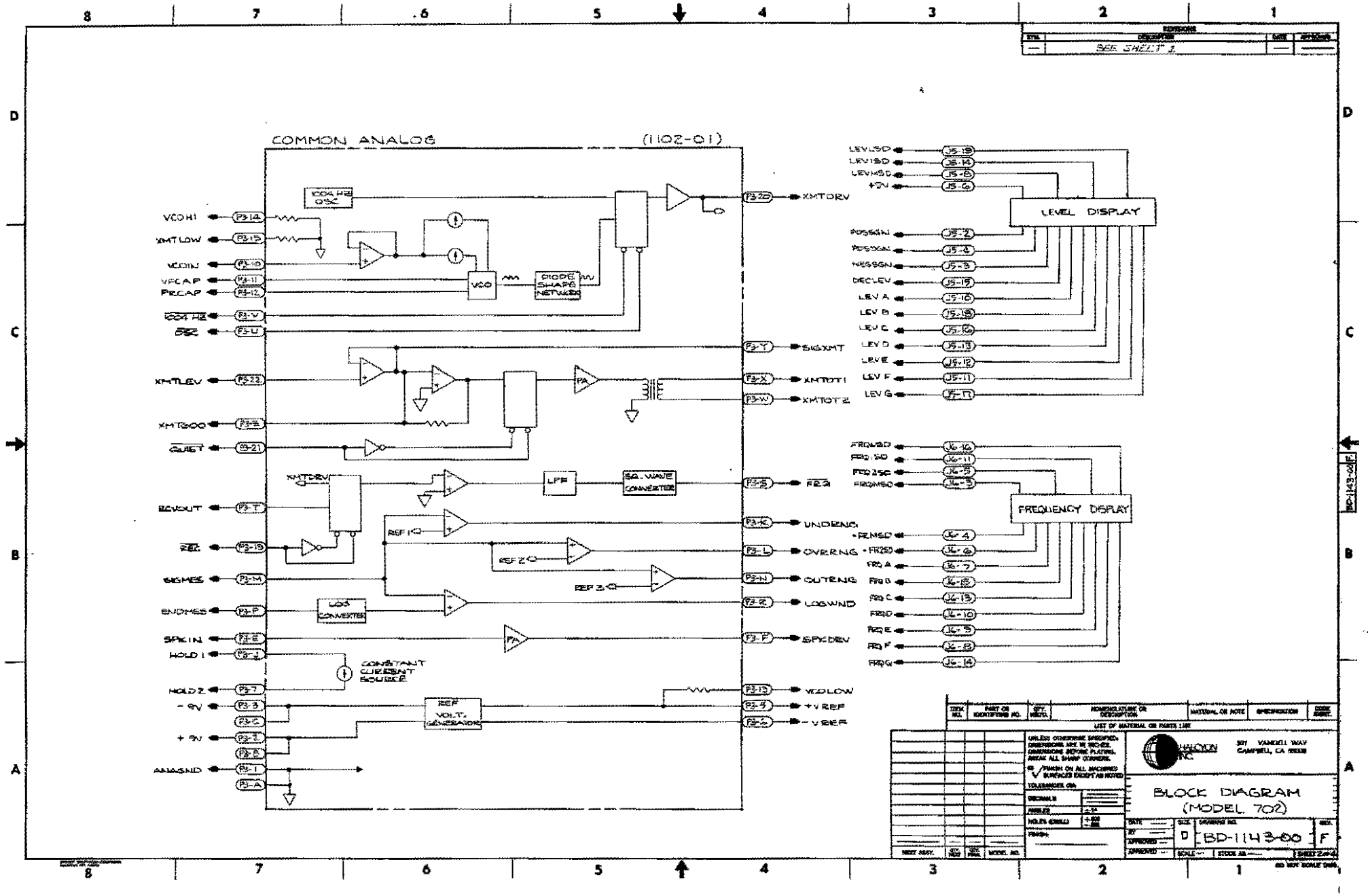
Top Assembly Drawings

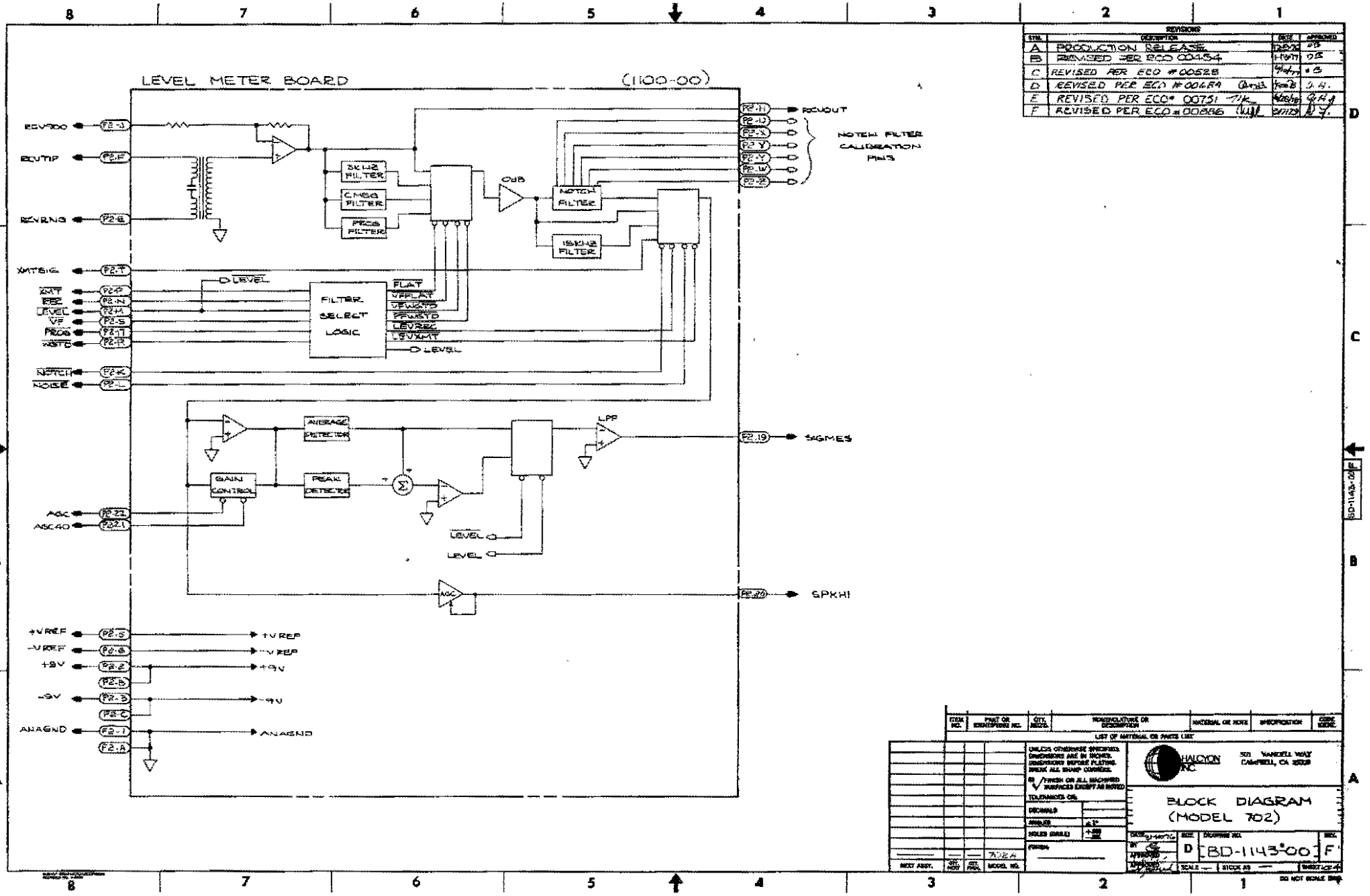
1136-00 701A Transmission Test Set
1143-00 702A Transmission Test Set

Sub-Assembly Drawings

0001-45 Enclosure, 701A
0002-45 Frequency Display, 702A
0002-46 Level Display, 702A
1057-00 DC/DC Converter, 702A
1057-15 DC/DC Conv Mod, 702A
1100-00 Level Meter*
1101-00 Digital Level*
1102-00 Common Analog, 701A
1102-01 Common Analog, 702A
1103-01 Mother Board, 701A
1104-00 Power Supply, 701A
1122-24 Front Panel, 701A
1122-25 Rear Panel, 701A
1143-01 Front Panel, 702A
1143-02 Inst Rack, 702A
1148-00 Mother Board, 702A
2084-01 Termination Board*

*Common to both 701A and 702A units


COMMON ANALOG (1102-01)
1004 HZ OSC
VCO
DIODE SHAPE NETWORK
PA
LPF
SQ. WAVE CONVERTER
LOG CONVERTER
CONSTANT CURRENT SOURCE
REF VOLT. GENERATOR
REF 1
REF 2
REF 3
VCOH1
XMTLOW
VCOIN
VFCAP
FRCAP
1004 HZ
OSC
XMTLEV
XMT600
QUIET
XMTDRV
RCVOUT
REF
SIGMES
ENDMES
SPKIN
HOLD 1
HOLD 2
- 9V
+ 9V
ANASND
XMTDRV
SIGXMT
XMTOT1
XMTOT2
FREQ
UNDRNG
OVRRNG
OUTRNG
LOGWND
SPKDRV
VCOLOW
+V REF
- V REF
LEVLSD
LEVISD
LEVMSD
+2V
LEVEL DISPLAY
POSSGN
POSSGN
NEGSGN
DEC LEV
LEV A
LEV B
LEV C
LEV D
LEV E
LEV F
LEV G
FRQMSD
FRQ 1SD
FRQ 2SD
FRQMSD
FREQUENCY DISPLAY
*FRMSD
*FR2SD
FRQ A
FRQ B
FRQ C
FRQD
FRQ E
FRQ F
FRQG
SEE SHEET 2
BD-1143-00F
HALCYON INC.
BLOCK DIAGRAM (MODEL 702)
BD-1143-00
F



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B	REVISED PER ECO 00454	1-19-81	DB
C	REVISED PER ECO #00528	4/14/82	J.B.
D	REVISED PER ECO #00689	6/28/83	J.H.
E	REVISED PER ECO# 00751	7/16/84	DB
F	REVISED PER ECO # 00886	8/17/87	DB

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LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

63 √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON:

DECIMALS

ANGLES ±1°

HOLES (DRILL) +.003 -.000

FINISH

NEXT ASSY. | QTY. REQD. | QTY. REQ. | MODEL NO. 702A

HALCYON INC. 505 YARNELL WAY CAMPBELL, CA 95008

BLOCK DIAGRAM (MODEL 702)

DRAWN | CHECKED | APPROVED | DATE

SIZE D | DRAWING NO. BD-1143-00 | REV. F

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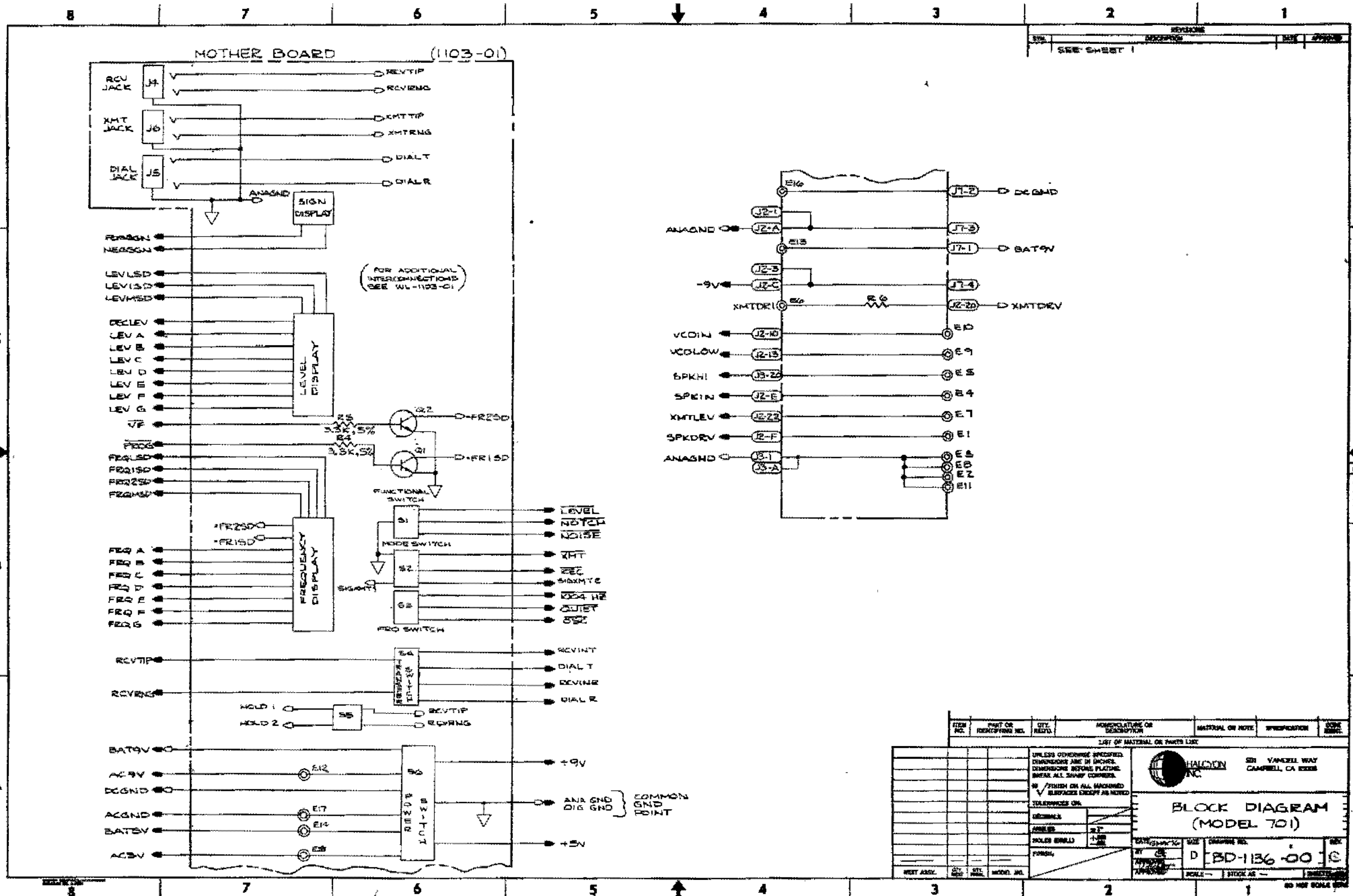
DO NOT SCALE PRINT

BD-1143-00F



MOTHER BOARD
(1103-01)
RCV JACK
J4
XMT JACK
J6
DIAL JACK
J5
RCVTIP
RCVRNG
XMTTIP
XMTRNG
DIAL T
DIAL R
ANAGND
SIGN DISPLAY
POSSGN
NEGSGN
LEVLSD
LEV1SD
LEVMSD
(FOR ADDITIONAL INTERCONNECTIONS SEE WL-1103-01)
DECLEV
LEV A
LEV B
LEV C
LEV D
LEV E
LEV F
LEV G
LEVEL DISPLAY
VF
R5 3.3K,5%
R4 3.3K,5%
Q2
Q1
+FR2SD
+FR1SD
FREQ
FRQLSD
FRQ1SD
FRQ2SD
FRQMSD
FUNCTIONAL SWITCH
+FR2SD
+FR1SD
FREQUENCY DISPLAY
FRQ A
FRQ B
FRQ C
FRQ D
FRQ E
FRQ F
FRQ G
S1
MODE SWITCH
S2
S3
SIGXMTE
FRQ SWITCH
LEVEL
NOTCH
NOISE
XMT
REC
1004 HZ
QUIET
OSC
RCVTIP
RCVRNG
S4
RCVINT
DIAL T
RCVINR
DIAL R
HOLD 1
HOLD 2
S5
RCVTIP
RCVRNG
BAT9V
AC9V
E12
DCGND
ACGND
E17
BAT5V
E14
AC5V
E18
S6
POWER SWITCH
+9V
ANA GND
DIG GND
COMMON GND POINT
+5V
E16
J1-2
DCGND
J2-1
ANAGND
J2-A
J1-3
E13
J1-1
BAT9V
J2-3
-9V
J2-C
J1-4
XMTDR1
E6
R6
J2-20
XMTDRV
VCOIN
J2-10
E10
VCOLOW
J2-13
E9
SPKHI
J3-20
E5
SPKIN
J2-E
E4
XMTLEV
J2-23
E7
SPKDRV
J2-F
E1
ANAGND
J3-1
J3-A
E3
E8
E2
E11
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HALCYON INC.
BLOCK DIAGRAM (MODEL 701)
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BD-1136-00
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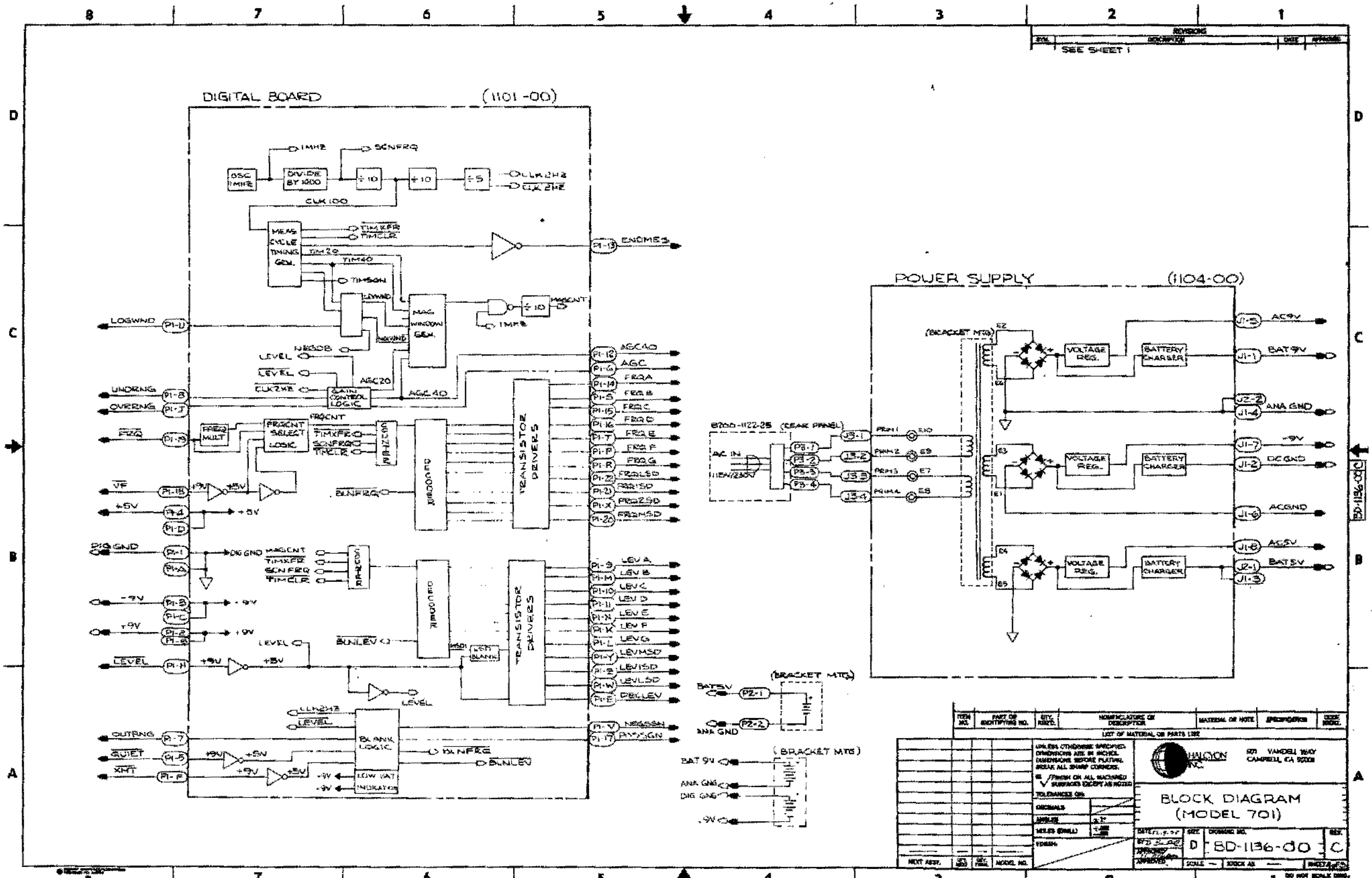
REVISIONS
SEE SHEET 1
DIGITAL BOARD
(1101-00)
OSC 1MHZ
DIVIDE BY 1000
÷10
÷10
÷5
1MHZ
SCNFRQ
CLK100
MEAS CYCLE TIMING GEN.
TIMXFR
TIMCLR
TIM20
TIM40
TIMSGN
ENDMES
MAG WINDOW GEN.
MAGCNT
LOGWND
NEGSDB
LEVEL
CLK2HZ
GAIN CONTROL LOGIC
AGC20
AGC40
AGC
UNDRNG
OVERNG
FRQ
FREQ MULT
FRQCNT
FREQCNT SELECT LOGIC
TIMXFRQ
SCNFRQ
TIMCLR
BLNFRQ
DECODER
TRANSISTOR DRIVERS
FRQA
FRQB
FRQC
FRQD
FRQE
FRQF
FRQG
FRQLSD
FRQ1SD
FRQ2SD
FRQMSD
VF
+5V
DIG GND
-9V
+9V
LEVEL
BLNLEV
LEV A
LEV B
LEV C
LEV D
LEV E
LEV F
LEV G
LEVMSD
LEV1SD
LEVLSD
PBCLEV
BLANK LOGIC
BLNFRQ
BLNLEV
NEGSGN
OUTRNG
QUIET
XMT
LOW BAT INDICATOR
POWER SUPPLY
(1104-00)
(BRACKET MTG)
8200-1122-25 (REAR PANEL)
AC IN
115V/230V
PRM1
PRM2
PRM3
PRM4
VOLTAGE REG.
BATTERY CHARGER
AC9V
BAT9V
ANA GND
-9V
DC GND
ACGND
AC5V
BAT5V
BAT5V
ANA GND
BAT 9V
DIG GND
-9V
BLOCK DIAGRAM
(MODEL 701)
HALCYON INC.
BD-1136-00
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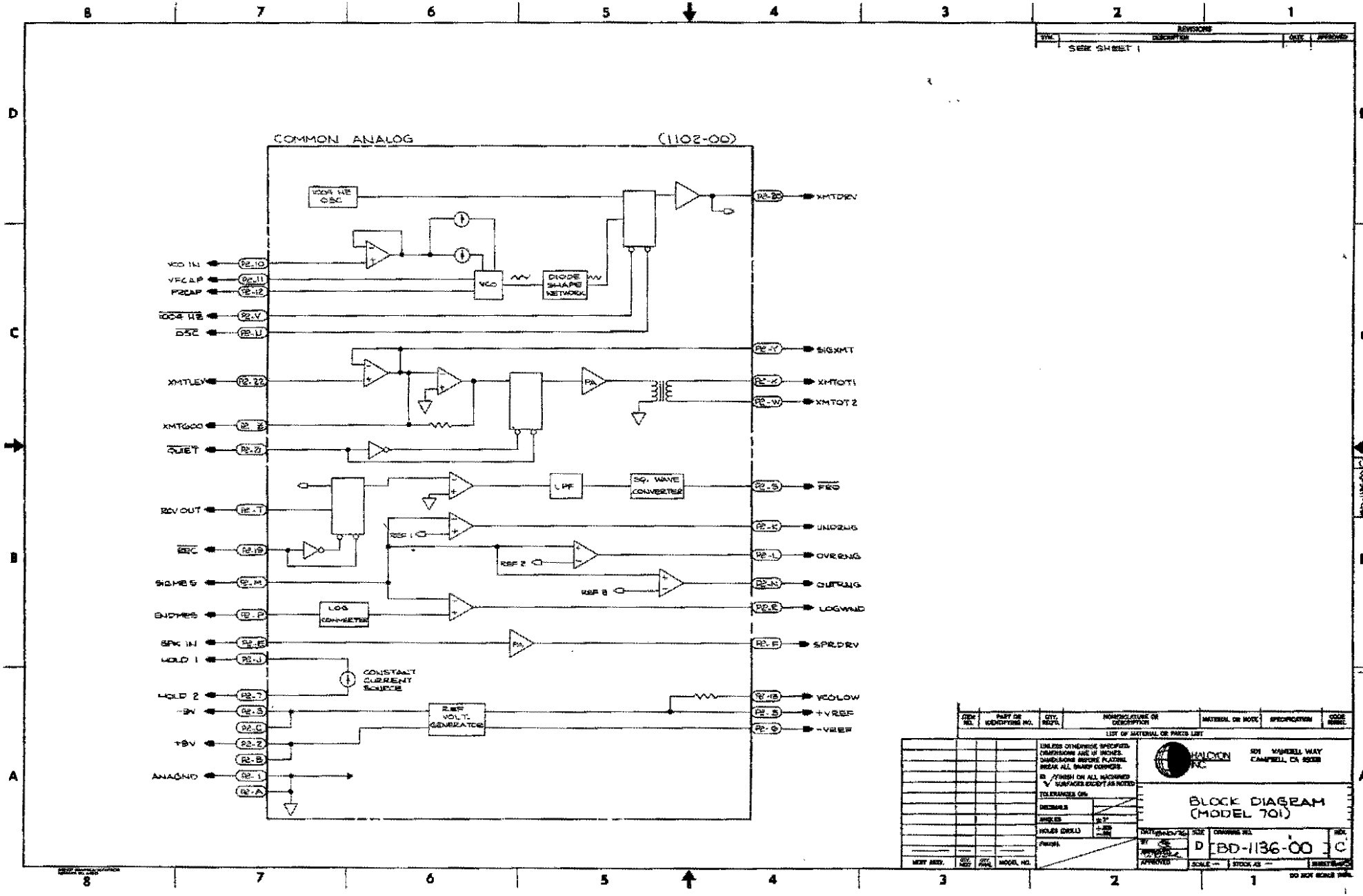
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P2CAP
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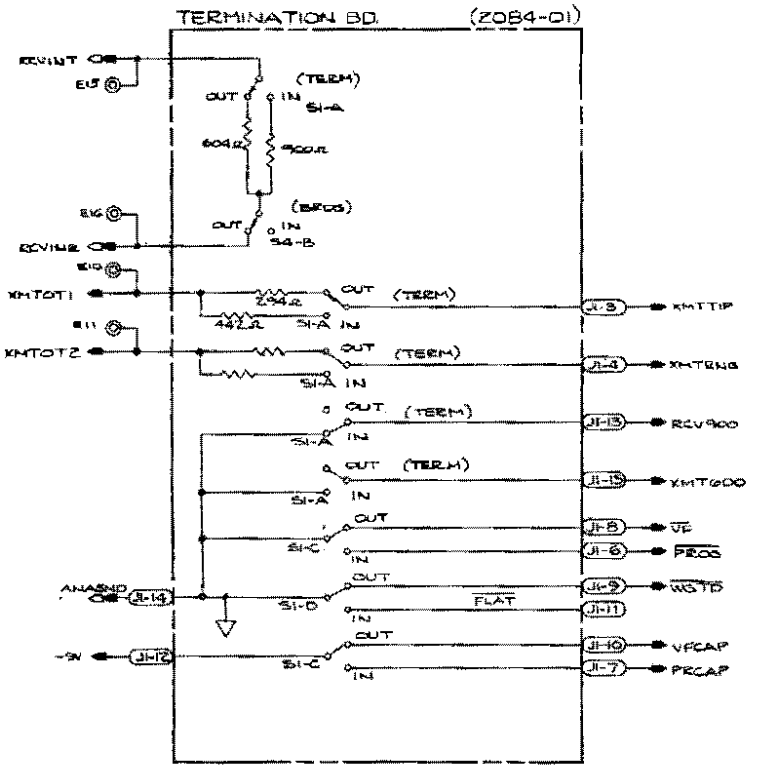
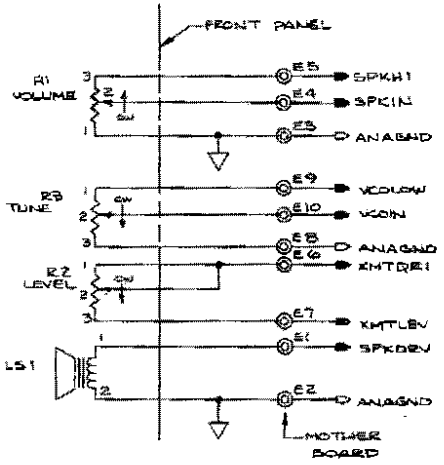
DSZ
XMTLEV
XMTGOOD
QUIET
RCV OUT
REC
SIGMES
ENDMES
SPK IN
HOLD 1
HOLD 2
-8V
+8V
ANAGND
VCO
DIODE SHAPE NETWORK
PA
LPF
SQ. WAVE CONVERTER
REF 1
REF 2
REF 3
LOG CONVERTER
CONSTANT CURRENT SOURCE
REF VOLT. GENERATOR
XMTDRV
SIGXMT
XMTOT1
XMTOT 2
REC
UNDRNG
OVRRNG
QUTRNG
LOGWND
SPKDRV
VCOLOW
+VREF
-VREF
HALCYON INC.
501 YARRELL WAY
CAMPBELL, CA 95008
BLOCK DIAGRAM
(MODEL 701)
BD-1136-00
D
C





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REVISIONS

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LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON:
DECIMALS
ANGLES ±1°
HOLES SHOULD ±.010
FINISH

NEXT ASSY. | USED ON | MODEL NO.

Wilcom Inc.
801 VANDELL WAY
CAMPBELL CA 95008

BLOCK DIAGRAM (MODEL 701)

SIZE D | DRAWING NO. BD-1136-00 | REV. E

SCALE — | SHEET 2 OF 2

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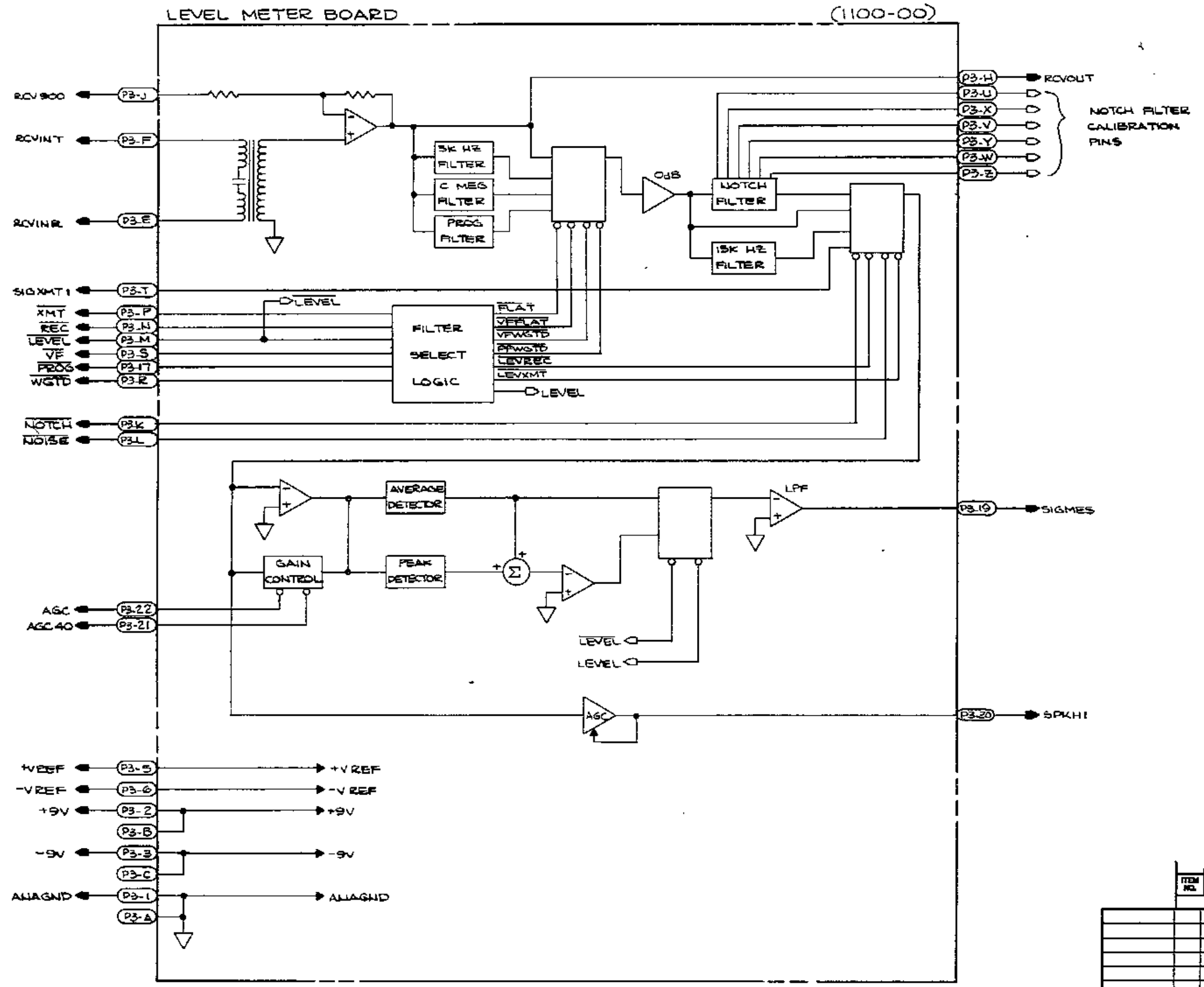
C	REVISED PER ECO # 00875		



LIST OF MATERIAL OR PARTS LIST

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HALCYON INC.
SUN VANDELL WAY
CAMPBELL, CA

BLOCK DIAGRAM
(MODEL 701)

SIZE: D
DRAWING NO.: BD-1136-00
REV.: C

PT-1136-06 REF 701A

DO NOT SCALE DWG.

REVISIONS			
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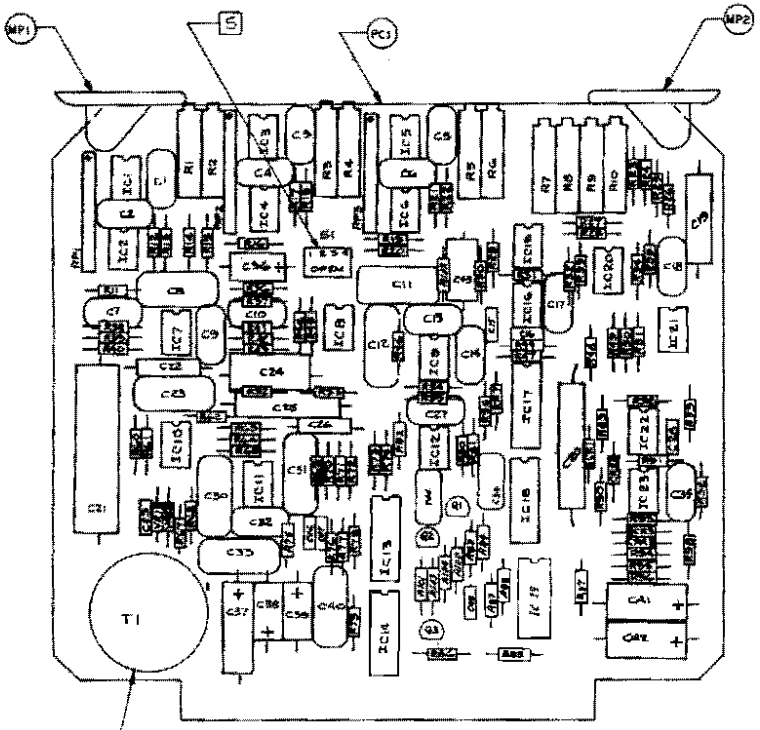

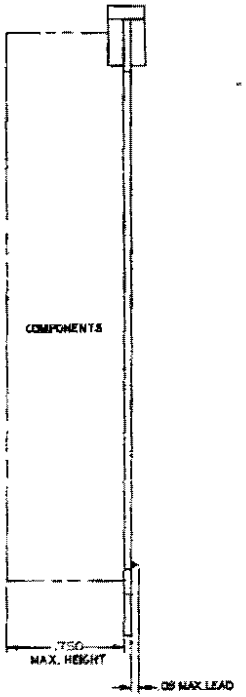

ITEM NO.	PART OR IDENTIFYING NO.	QTY REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

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J-1145-01	1	—	701 A	
ED-1100-16	1	—	701 A	
ED-1100-16	1	—	701 A	

NEXT ASSY	QTY REQ'D	QTY SERIAL	MODEL NO

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

63 √ FINISH ON ALL MACHINED √ SURFACES EXCEPT AS NOTED

TOLERANCES ON:

DECIMALS

ANGLES ±1°

HOLES (DRILL)

FINISH

SEE NOTES

HALCYON INC. 501 – WANDELL WAY CAMPBELL, CA 95008

PCB ASSEMBLY- LEVEL METER BD.

DATE 3-9-79 | SIZE D | DRAWING NO ED-1100-00 | REV C

SCALE 2:1 | STOCK AS SHOWN | SHEET 1 OF 1

DO NOT SCALE DWG

[5] T1 & S1 TO BE HAND-SOLDERED. DO NOT IMMERSE IN SOLVENT

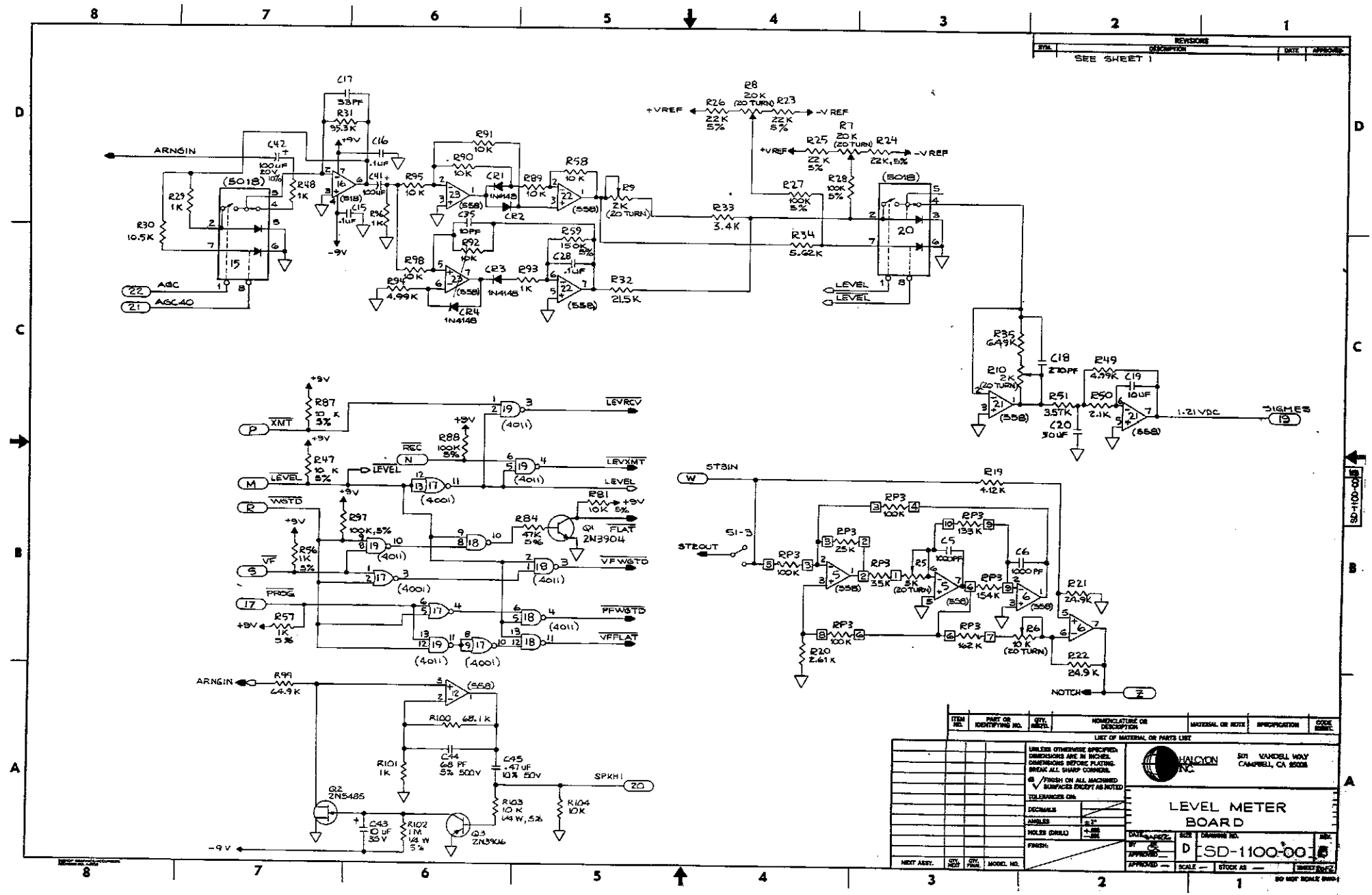
4. FOR PERFORMANCE SPEC. SEE X-1100-00

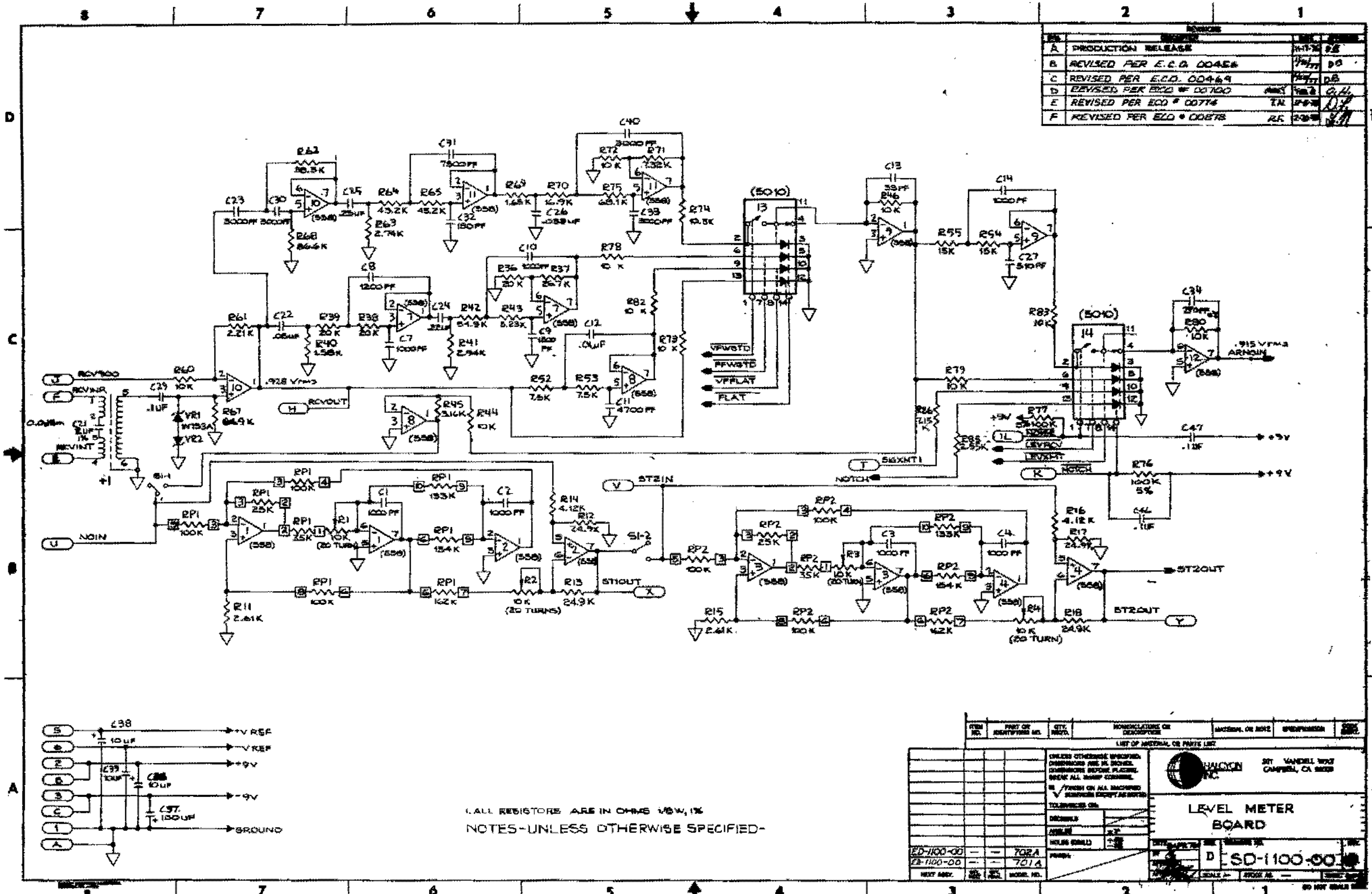
3. ■ SQUARE PADS DENOTES CATHODE END OF DIODE, POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET

2. FOR LIST OF MATERIALS SEE 8000-1100-00

1. FOR SCHEMATIC SEE SD-1100-00

NOTES – UNLESS OTHERWISE SPECIFIED:


REVISIONS
SEE SHEET 1
ARNGIN
AGC
AGCAO
LEVEL
LEVEL
+VREF
-VREF
+VREF
-VREF
1.21 VDC
SIGMES
STBIN
STEOUT
SI-3
NOTCH
SPKH1
XMT
REC
LEVEL
WGTD
VF
PROG
LEVRCV
LEVXMT
LEVEL
FLAT
VFWGTD
PFWGTD
VFFLAT
LEVEL METER BOARD
HALCYON INC.
501 VANDELL WAY CAMPBELL, CA 95008
SIZE D
DRAWING NO. SD-1100-0010
REV. B
SCALE —
SHEET 1 OF 2
DO NOT SCALE DRAWING

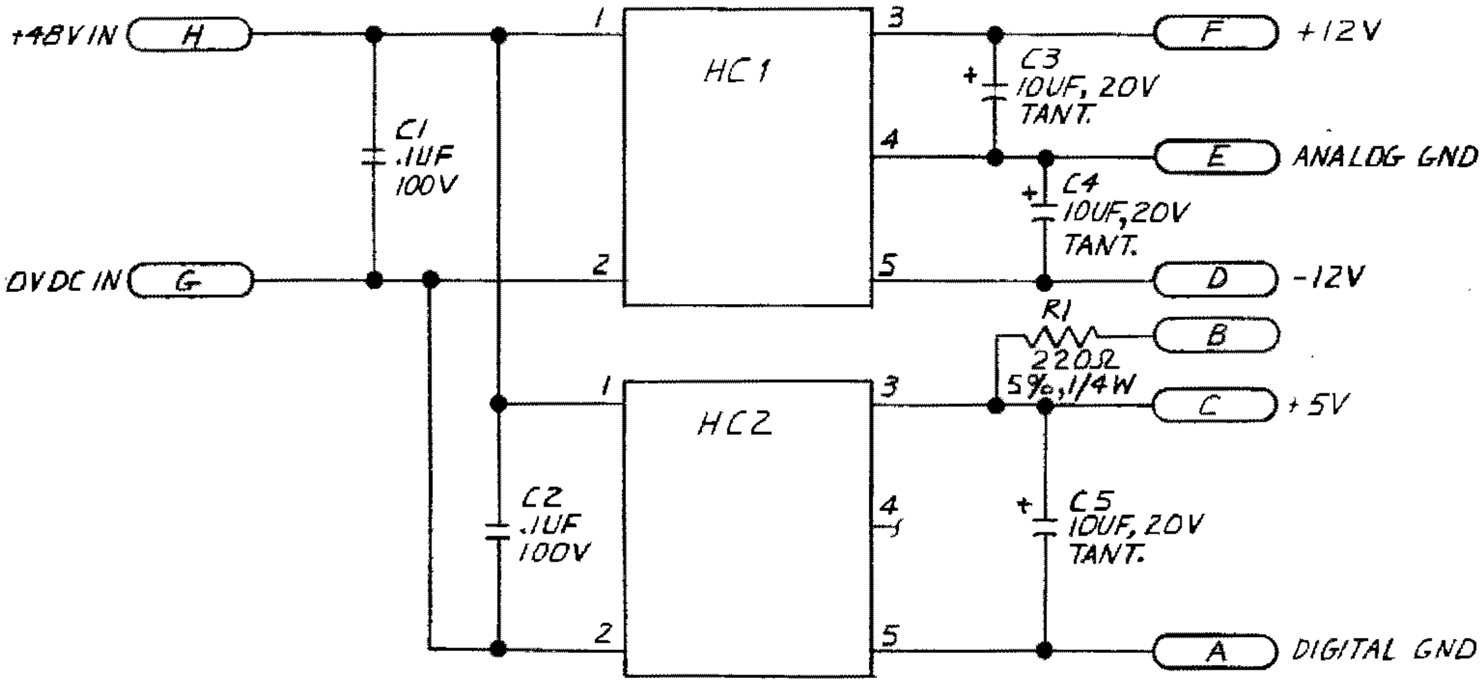


PRODUCTION RELEASE
REVISED PER E.C.O. 00456
REVISED PER E.C.O. 00469
REVISED PER ECO # 00700
REVISED PER ECO # 00774
REVISED PER ECO # 00878
RCV500
RCVINR
RCVINT
RCVOUT
NOIN
ST1OUT
ST2IN
ST2OUT
SIGXNT1
NOTCH
VFWGTD
FFWGTD
VFFLAT
FLAT
ARNOIN
.928 Vrms
.915 Vrms
+V REF
-V REF
+9V
-9V
GROUND
ALL RESISTORS ARE IN OHMS 1/8W, 1%
NOTES-UNLESS OTHERWISE SPECIFIED-
HALCYON INC.
LEVEL METER BOARD
SD-1100-00

DWG. NO. SD-1057-00 | SH 1 | REV. A

REVISIONS

REV.	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	3-6-78	[illegible]



1. FOR INTERCONNECTION WIRE LIST SEE WL-1057-15.

NOTES - UNLESS OTHERWISE SPECIFIED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION

PARTS LIST

ED-1057-00	702A MOD
NEXT ASSY	
APPLICATION	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH: SEE NOTES

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS		DATE
DRAWN	LONG. N	3-6-78
CHECKED	[illegible]	3-6-[illegible]
ISSUED	[illegible]	[illegible]
	[signature]	3/8/78

HALCYON INC.

DC/DC CONVERTER BD

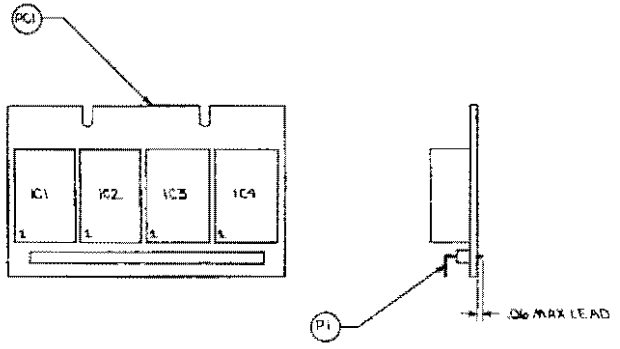
SIZE: B | FSCM NO. | DWG. NO.: SD-1057-00 | REV.: A

SCALE: NONE | SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1184

ED-0002-46	P1	C

ZONE	REV	DESCRIPTION	DATE	APPROVED
	C	REVISED PER ECO #00816 JKS	12-18-78	



5. MOUNT IC'S WITH PIN #1 AT POSITION SHOWN (SQUARE PADS).

A. A. SOLDERING (LEAD TEMP & SOLDERING TIME FOR IC1 THRU IC4 SHALL NOT EXCEED 230°C FOR 5 SECONDS (WITHOUT PRE HEATING).
   L. AT NO TIME DURING THE ASSY. PROCESS (EG. A COMBINATION OF PRE HEATING PRIOR TO SOLDERING) SHALL THE INTERNAL TEMPERATURE EXCEED 85°C.
   B. CLEANING: ONLY THE FOLLOWING CLEANING SOLUTIONS ARE TOLERABLE: FREON TF, ISOPROPYL ALCOHOL OR WATER.
   L. DO NOT IMMERSE HEATED ASSY IN CLEANING SOLUTION.

3. PINS TO PROTRUDE .06 MAX. FROM BACKSIDE OF PCB.
2. FOR LIST OF MATERIALS SEE BOM ED-0002-46.
1. FOR SCHEMATIC SEE ED-0002-46.

NOTES UNLESS OTHERWISE SPECIFIED:

9000-1143-00	702
NEXT ASSY	USED ON
APPLICATION	

SEE NOTES

DO NOT SCALE DRAWING

APPROVALS	DATE
JKS	12-18-78
	1-9-79
	1-9-79

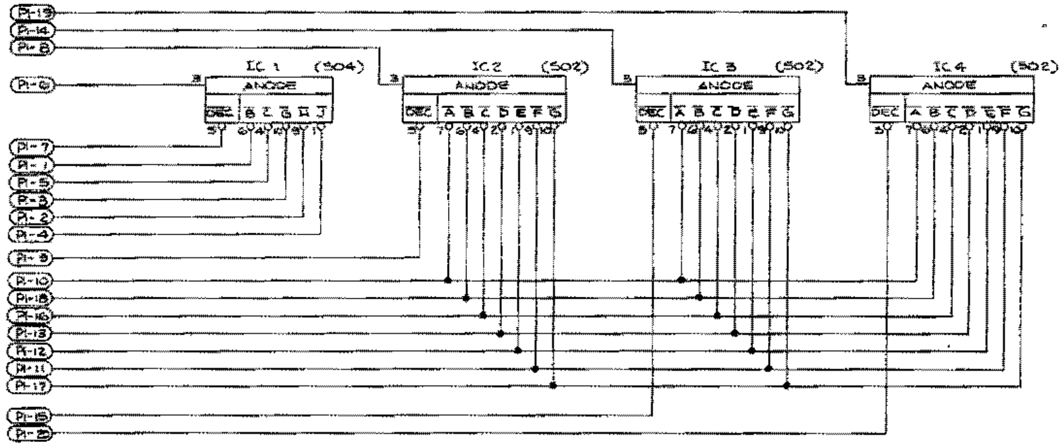
PARTS LIST

PCB ASSY.
LEVEL DISPLAY

SIZE	DRAWING NO	REV
D	ED-0002-46	C

SCALE: 2/1 | STOCK AS: 2000 | SHEET 1 OF 1

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE		



1 FOR MAT'L LIST SEE 8000-0002-46

NOTES - UNLESS OTHERWISE SPECIFIED

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

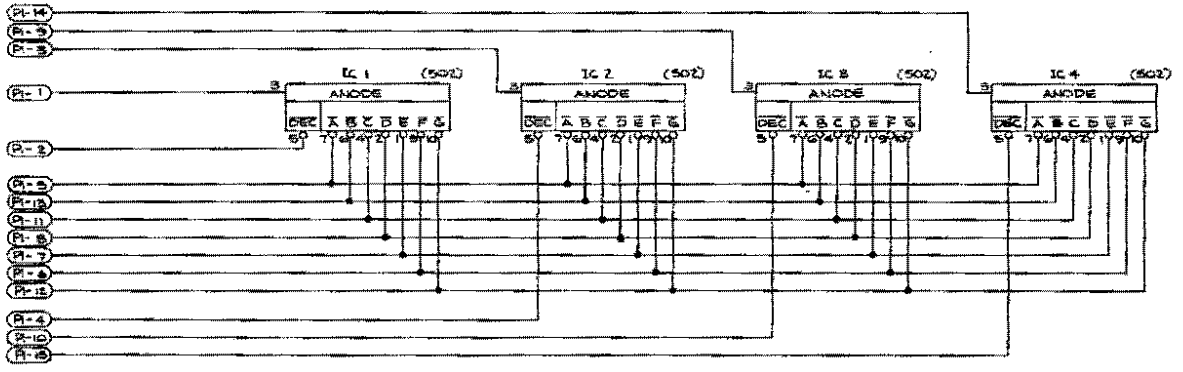
HALCYON INC.
501 VANDELL WAY
CAMPBELL, CA

LEVEL
DISPLAY BOARD

SIZE D
DRAWING NO. SD-0002-46
REV. A

NEXT ASSY. | MODEL NO. | SCALE | FINISH

DO NOT SCALE DWG.



1. FOR MATL LIST SEE 8000-0002-45

NOTES- UNLESS OTHERWISE SPECIFIED

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	12-6-72	

HALCYON INC. 201 VINDELL WAY CAMPBELL, CA. 95008

FREQUENCY DISPLAY BOARD-702

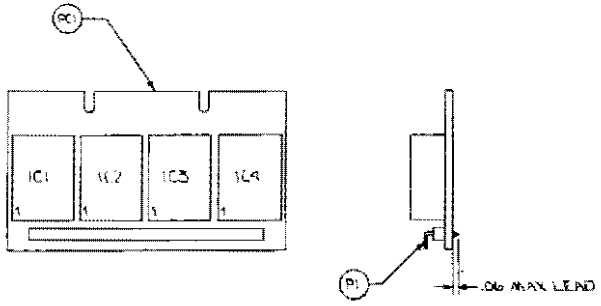
DRAWING NO. D SD-0002-45 REV. A

SCALE — STOCK NO. —

DWG NO	SIZE	REV
ED-0002-45	D	C

REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
—	C	REVISED PER ECO #00816 JKS	12-18-78	



5. MOUNT ICS WITH PIN #1 IN POSITION SHOWN (SQUARE PAD).
4. A. SOLDERING: LEAD TEMP & SOLDERING TIME FOR IC1 THRU IC4 SHALL NOT EXCEED 230°C FOR 5 SECONDS (WITHOUT PRE HEATING).
   I. AT NO TIME DURING THE ASSY PROCESS (E.G. A COMBINATION OF PRE HEATING PRIOR TO SOLDERING) SHALL THE INTERNAL TEMPERATURE OF A DEVICE EXCEED 85°C.
   B. CLEANING: ONLY THE FOLLOWING CLEANING SYSTEMS ARE PERMISSABLE: FREON TF, ISOPROPYL ALCOHOL, OR WATER.
      I. DO NOT IMMERSE HEATED ASSY IN COLD CLEANING SOLUTION.
3. PINS TO PROTRUDE .06 MAX FROM BACKSIDE OF PCB.
2. FOR LIST OF MATERIALS SEE WWII FOLDER.
1. FOR SCHEMATIC SEE SD-0002-45.

NOTES: UNLESS OTHERWISE SPECIFIED:

8000-1193-00	702					
NEXT ASSY	USED ON	SEE NOTES				
APPLICATION		DO NOT SCALE DRAWING				

QTY	ZONE	REV	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL SPECIFICATION
				PARTS LIST	

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. TOLERANCES ARE: FRACTIONS ±; DECIMALS .X ±, .XX ±, ANGLES ±

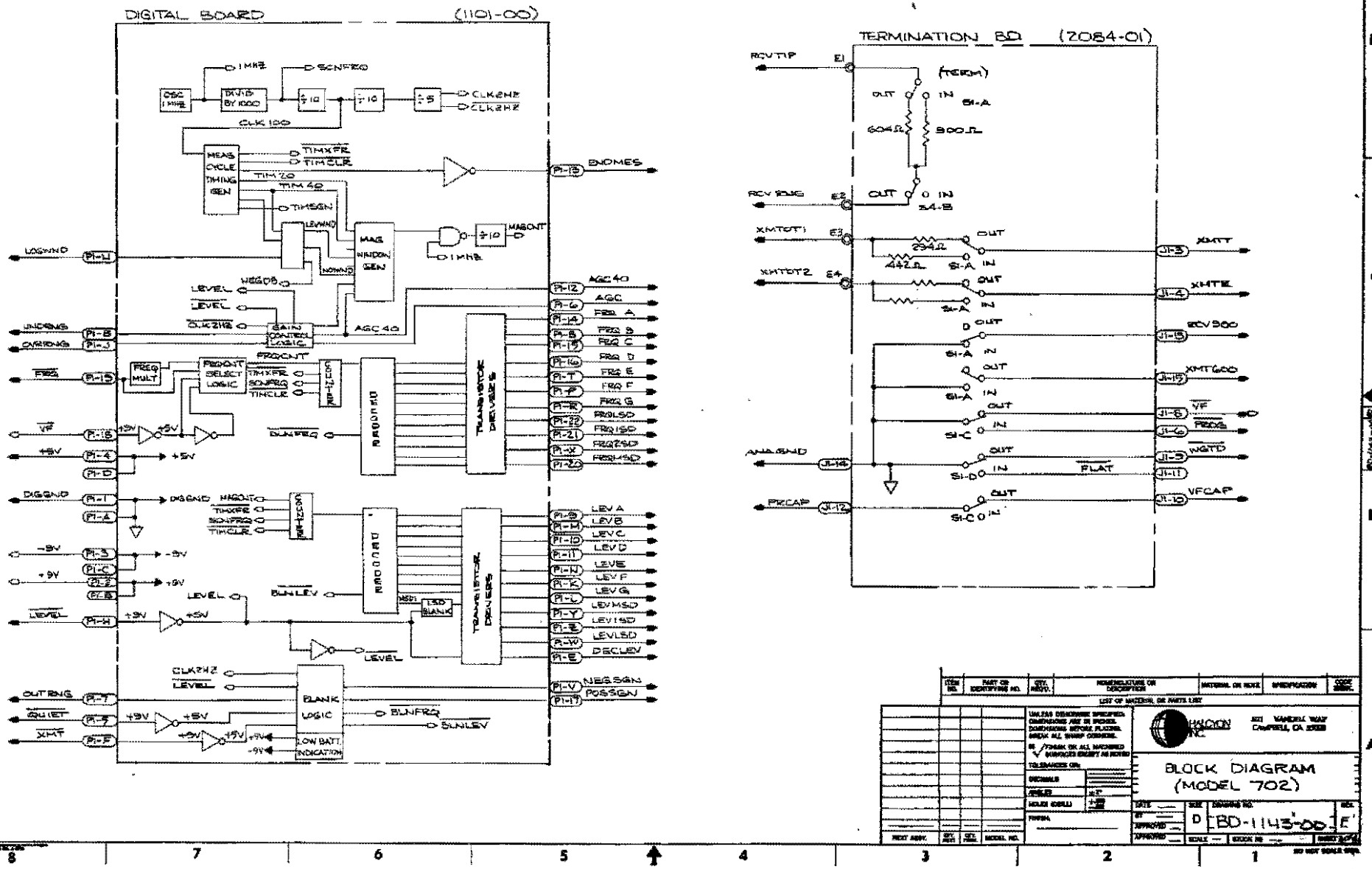
	APPROVALS	DATE
DRAWN	[illegible]	12-18-78
CHECKED	Jim Bagg	1-9-79
ENGINEER	[illegible]	1-9-79
PROJECT MGR	[illegible]	1/9/79

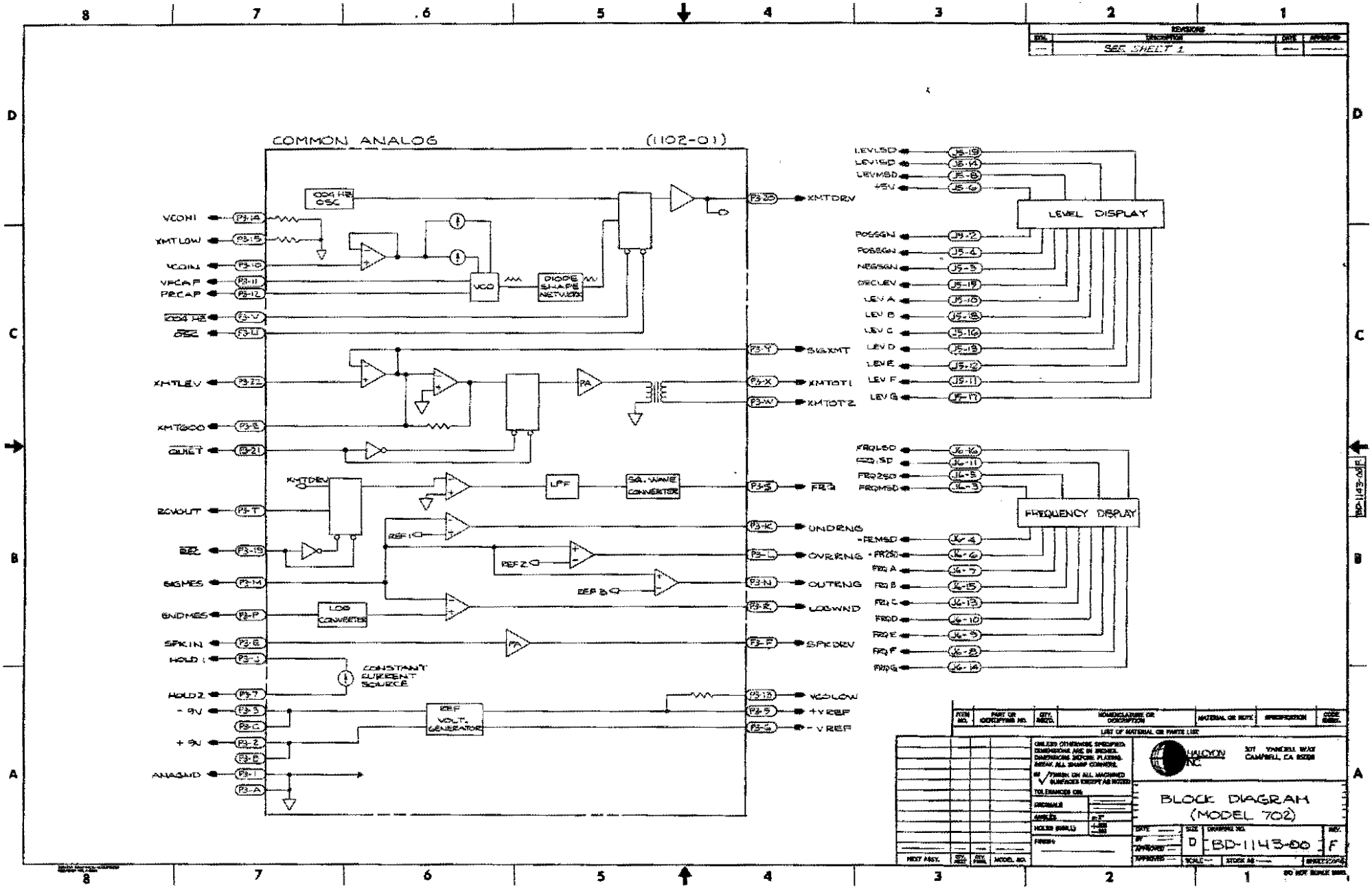
COMPONENT NO

PCB ASSEMBLY FREQUENCY DISPLAY

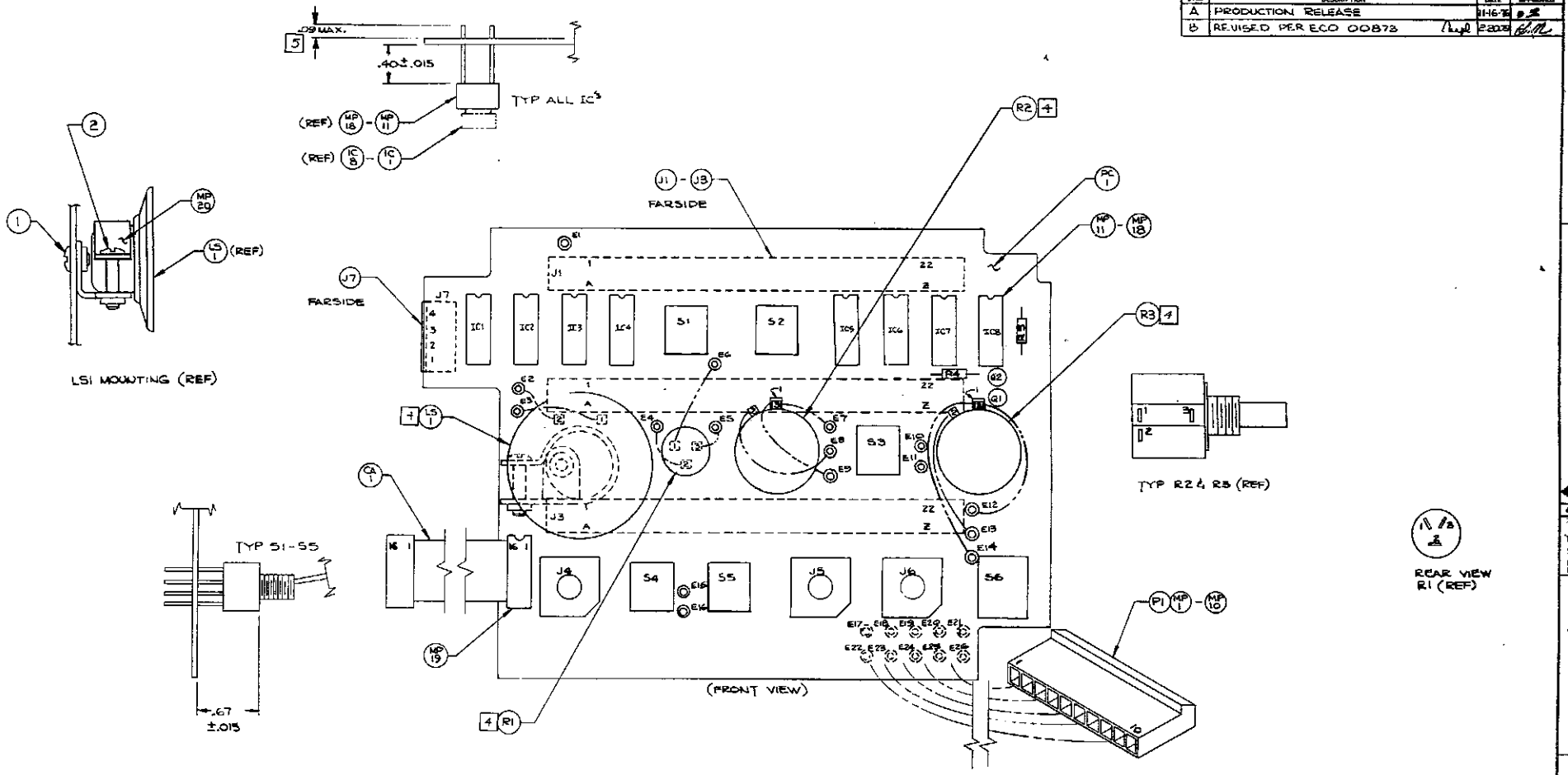
SIZE	DRAWING NO	REV
D	ED-0002-45	C

DRAWING IS STOCK AS: 8000 SHEET 1 OF 1


DIGITAL BOARD (1101-00)
TERMINATION BD (2084-01)
REVISIONS
SEE SHEET 1
1MHZ
SCNFREQ
CLK2MHZ
CLK100
MEAS CYCLE TIMING GEN
TIMXFR
TIMCLR
TIM20
TIM40
TIMSGN
LSWND
NSWND
MAG WINDOW GEN
MAGOUT
AGC40
AGC
GAIN CONTROL LOGIC
FREQ MULT
FREQUENCY SELECT LOGIC
FREQUENCY SYNTHESIZER
TRANSMITTER DRIVERS
BLNFREQ
LEVEL
BLNLEV
LSD BLANK
BLANK LOGIC
LOW BATT. INDICATION
BLNFRQ
BLNLEV
LASWND
UNCRNG
CWRNG
FREQ
VF
+9V
DIGGND
-9V
OUTRNG
INLIET
XMT
ENDMES
NEGSGN
POSSGN
RCVTIP
RCVRING
XMTDT1
XMTDT2
ANAGND
PTCAP
TERM
IN
OUT
604Ω
900Ω
294Ω
442Ω
XMTT
XMTR
RCV900
XMT600
FLAT
VFCAP
BLOCK DIAGRAM (MODEL 702)
BD-1143-00
F


COMMON ANALOG (1102-01)
SEE SHEET 1
VCONT
XMT LOW
VCOIN
VRCAP
PRCAP
1004 HZ
OSC
XMTLEV
XMTSCO
QUIET
RCVOUT
SIGMES
GNDMES
SPKIN
HOLD
HOLD2
- 9V
+ 9V
ANAGND
1004 HZ OSC
VCO
DIODE SHAPE NETWORK
PA
LPF
SA. WAVE CONVERTER
LOG CONVERTER
CONSTANT CURRENT SOURCE
REF VOLT. GENERATOR
XMTDRV
SIGXMT
XMTOT1
XMTOT2
FRQ
UNDRNG
OVRRNG
OUTRNG
LOGWND
SPKDRV
VCOLOW
+VREF
-VREF
LEVEL DISPLAY
FREQUENCY DISPLAY
HALCYON INC.
BLOCK DIAGRAM (MODEL 702)
BD-1143-00
D
F

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	11-16-76	
B	REVISED PER ECO 00873	2-2078	



5 MAXIMUM LEAD LENGTH FOR ALL LEADS ON PAB SIDE TO BE .09.

4 FOR MOUNTING AND INSTALLATION ADJUSTMENTS SEE DWG. ED-1122-24

3. FOR SCHEMATIC SEE SD-1103-01

2. FOR LIST OF MATERIALS SEE 8000-1103-01

1. FOR WIRING LIST SEE WL-1103-01

NOTES-UNLESS OTHERWISE SPECIFIED

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

63 √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON:

DECIMALS

ANGLES ± 1°

HOLES (DRILL) +.003 -.000

FINISH SEE NOTES

NEXT ASSY ED 1122 24 | QTY. REQ'D. 1 | QTY. PER ASSY | MODEL NO 701A

DATE 21 JUL 76

BY

APPROVED

APPROVED

SIZE D

DRAWING NO. ED-1103-01

REV. B

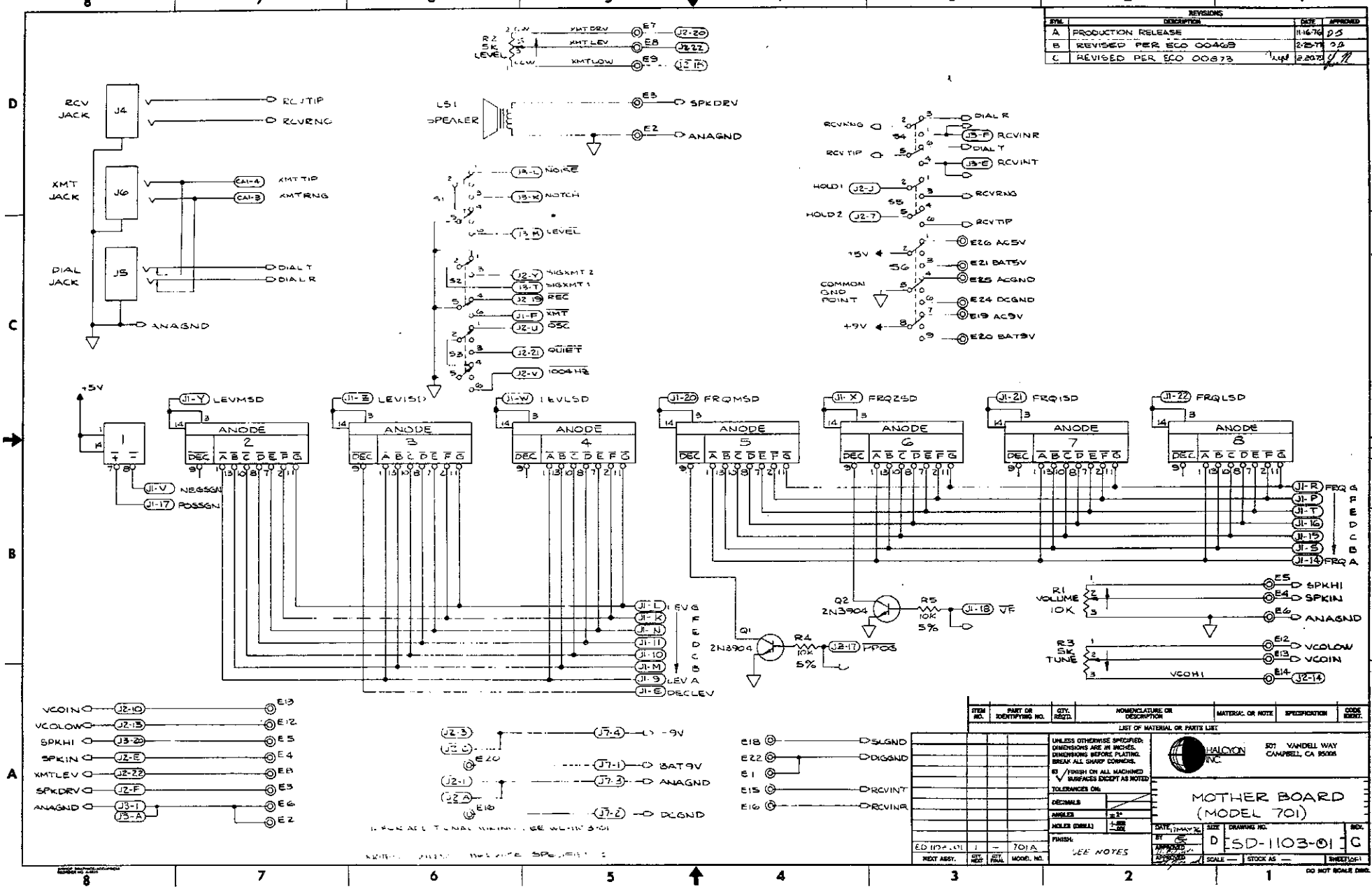
SCALE 2X

STOCK NO 8000

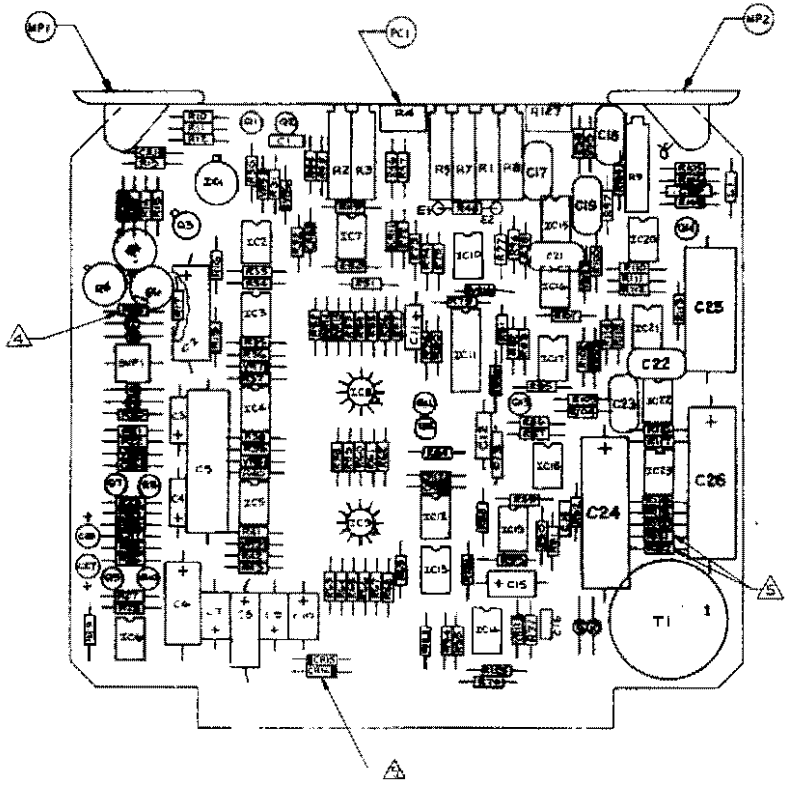
SHEET 1 of 4

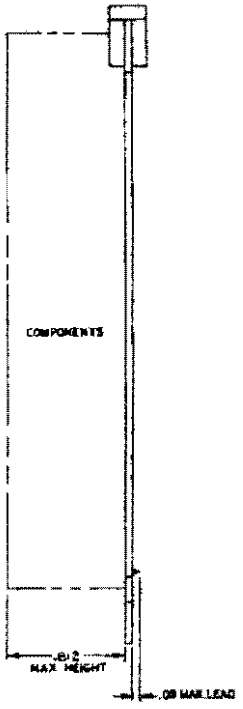
UNIVOYN INC. 501 VANDELL WAY CAMPBELL, CA 95008

PCB ASSEMBLY-
MOTHER BOARD(701)


REVISIONS
SYM | DESCRIPTION | DATE | APPROVED
A | PRODUCTION RELEASE | 11-16-76 | DS
B | REVISED PER ECO 00469 | 2-25-77 | DS
C | REVISED PER ECO 00873 | 2-20-78
RCV JACK J4
XMT JACK J6
DIAL JACK J5
RCVTIP
RCVRNG
XMTTIP
XMTRNG
DIAL T
DIAL R
ANAGND
LS1 SPEAKER
SPKDRV
XMTDRV
XMTLEV
XMTLOW
NOISE
NOTCH
LEVEL
SIGXMT 2
SIGXMT 1
REC
XMT
OSC
QUIET
1004 HZ
DIAL R
DIAL T
RCVINR
RCVINT
HOLD1
HOLD2
+5V
COMMON GND POINT
+9V
AC5V
BAT5V
AGND
DCGND
AC9V
BAT9V
LEVMSD
LEVLSD
FRQMSD
FRQLSD
ANODE
NEGSGN
POSSGN
VF
PPOS
VOLUME 10K
SPKHI
SPKLO
VCOLOW
VCOIN
VCOHI
SLGND
DIGGND
MOTHER BOARD (MODEL 701)
HALCYON INC.
501 VANDELL WAY
CAMPBELL, CA 95008
SIZE D
DRAWING NO. SD-1103-01
REV. C
SCALE —
SHEET 1 OF 1
DO NOT SCALE DWG.

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION PER ECO # 00528	4/1/91	MS





⚠4 DO NOT LOAD.

⚠5 INSULATE LEADS OF COMP R18 WITH TEFLON TUBING AND ENSURE THAT AN AIR GAP (MIN .03) EXIST BETWEEN Q4, Q5, AND Q6. IF NECESSARY, INSULATE WITH SHRINK TUBING.

1. SQUARE PADS DENOTES CATHODE END OF DIODE. POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET.
2. FOR LIST OF MATERIALS SEE 8000-1102-01
3. FOR SCHEMATIC SEE ED-1102-01

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	PART OR IDENTIFYING NO.	QTY REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE INDENT.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS. √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED. TOLERANCES ON: DECIMALS, ANGLES ±1°, HOLES (DRILL) ±.005 ±.003, Finish

HALCYON INC. 501 – SANDELL STAGE CAMPBELL, CA 95008

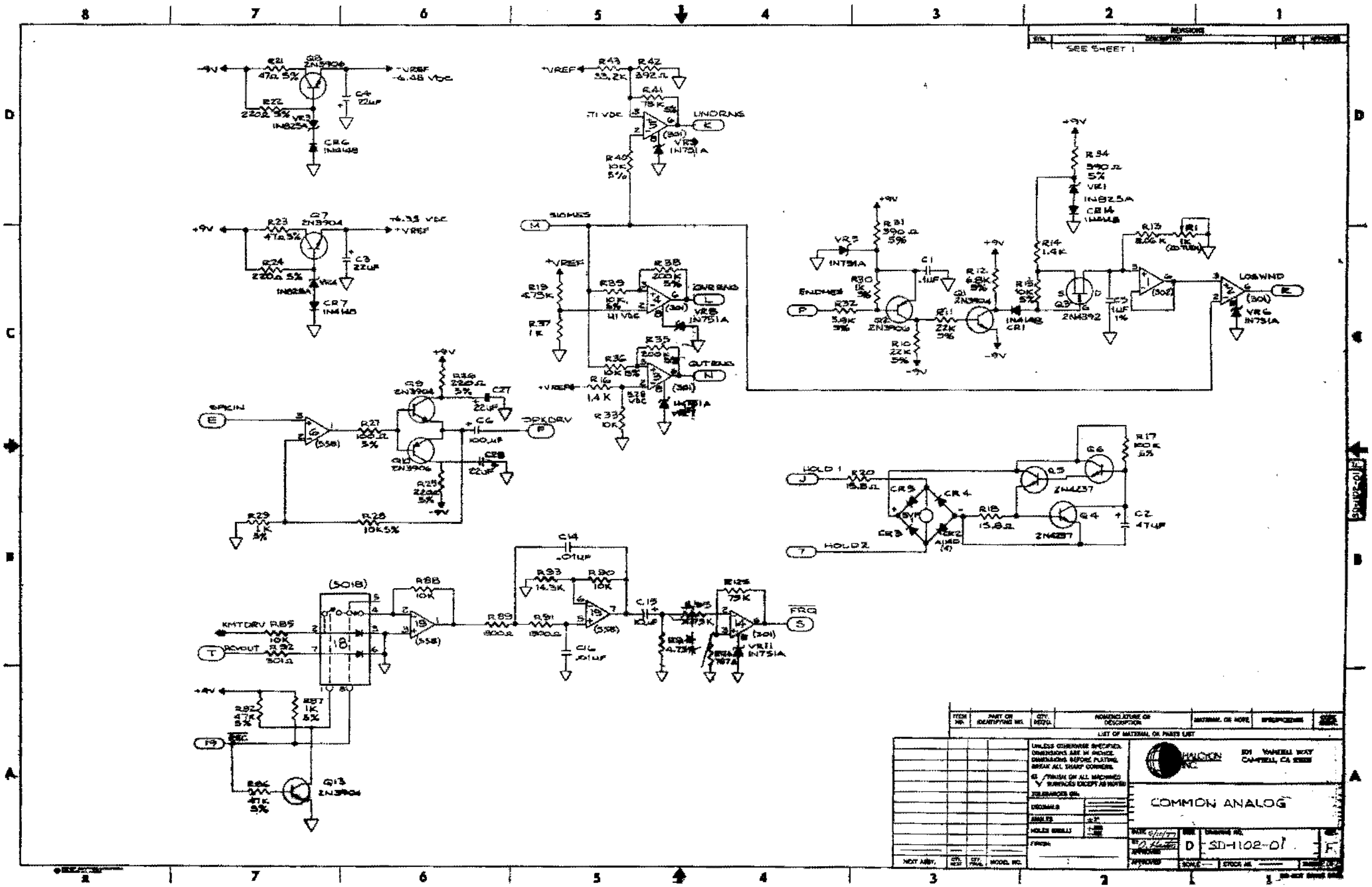
PCB ASSEMBLY– COMMON ANALOG

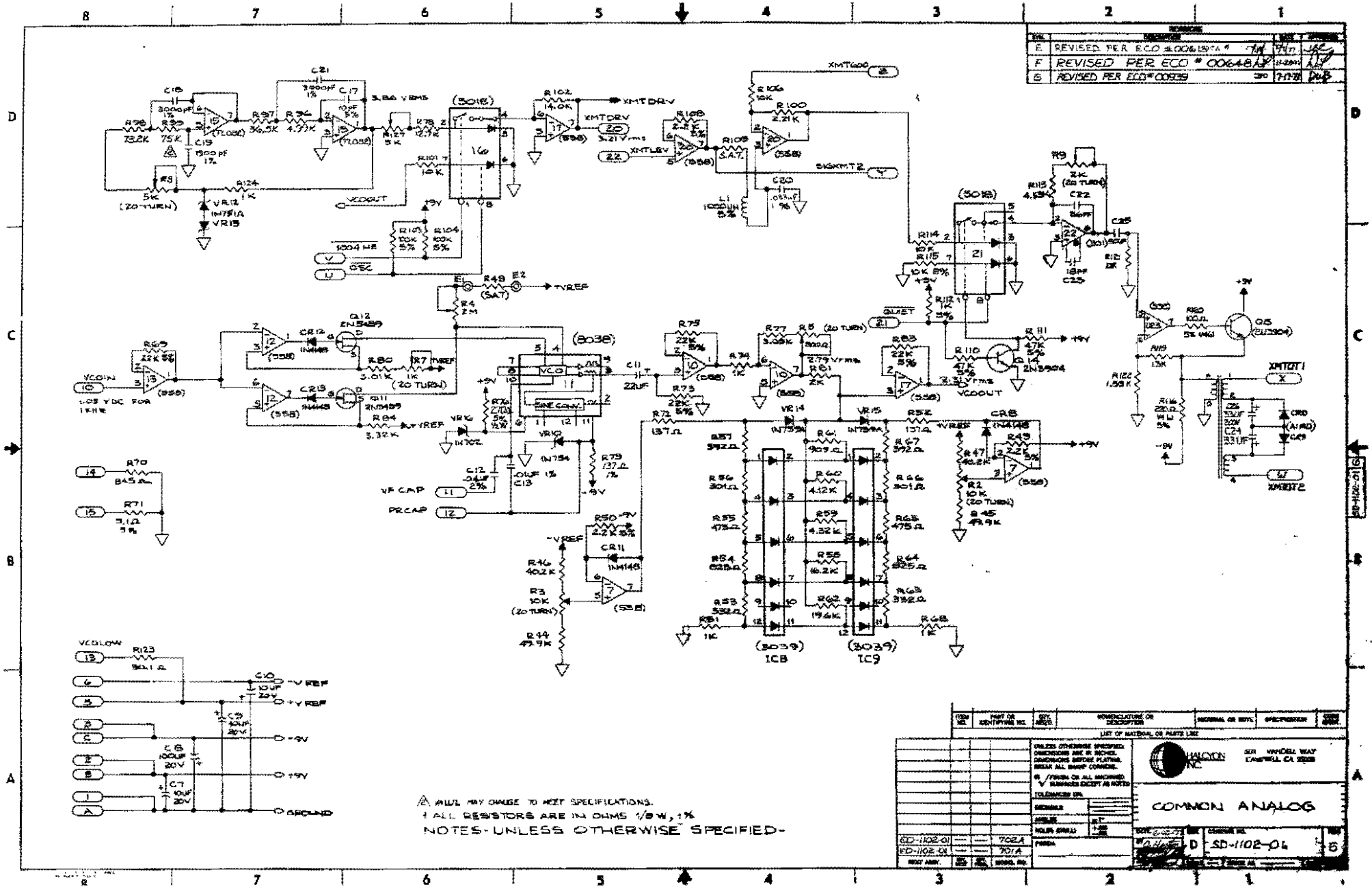
NEXT ASSY	QTY	UNIT	MODEL NO.

DATE	SIZE	DRAWING NO	REV.
4/1/91	D	ED-1102-01	A
	SCALE 2/1	STOCK AS 8000	SHEET 1 OF 1

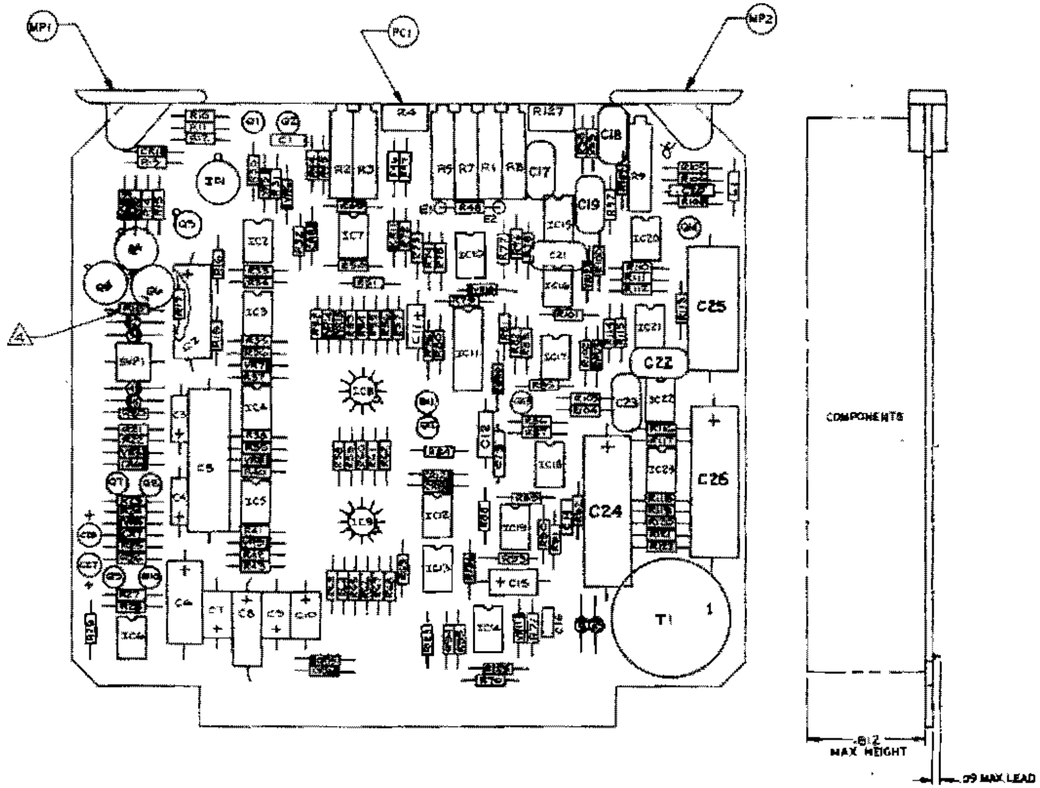
DO NOT SCALE DRAWING

ED-1102-01 A


REVISIONS
SEE SHEET 1
COMMON ANALOG
SD-1102-01
HALCYON INC.
101 VANDELL WAY CAMPBELL, CA
LIST OF MATERIAL OR PARTS LIST
+VREF 6.48 VDC
+4.35 VDC +VREF
UNDRNG
OVRRNG
OUTRNG
SIGMSS
ENGMET
LOSWND
HOLD 1
HOLD 2
SPKDRV
SPKIN
KMTDRV
RCVOUT
FRQ
2N3904
2N3906
2N4392
2N4237
IN751A
IN825A
IN4148


REVISED PER ECO # 00648
REVISED PER ECO # 00899
XMTDRV
XMTLEV
VCOOUT
VCOIN
VREF
+9V
-9V
+19V
GROUND
VCOLOW
VF CAP
PRECAP
SINE CONV
VCO
IC8
IC9
NOTES- UNLESS OTHERWISE SPECIFIED-
ALL RESISTORS ARE IN OHMS 1/8 W, 1%
ALL MAY CHANGE TO MEET SPECIFICATIONS.
COMMON ANALOG
SD-1102-04
ED-1102-01
ED-1102-02

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED
B	REVISED PER ECO 00465	[illegible]	DG
[illegible]	REVISED PER ECO 00485	[illegible]	[illegible]



⚠ INSULATE LEADS OF COMP R18 WITH TEFLON TUBING AND INSURE THAT AN AIR GAP (MIN .03) EXIST BETWEEN Q4, Q5, AND Q6. IF NECESSARY, INSULATE WITH SHRINK TUBING.

3. ▣ SQUARE PADS DENOTES CATHODE END OF DIODE, POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET

2. FOR LIST OF MATERIALS SEE 6000-1102-00

1. FOR SCHEMATIC SEE SD-1102-00

NOTES – UNLESS OTHERWISE SPECIFIED:

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON: DECIMALS | ANGLES ±1° | HOLES (DRILL)

FINISH:

HALCYON INC. 381 – VANDELL WAY CAMPBELL, CA 95008

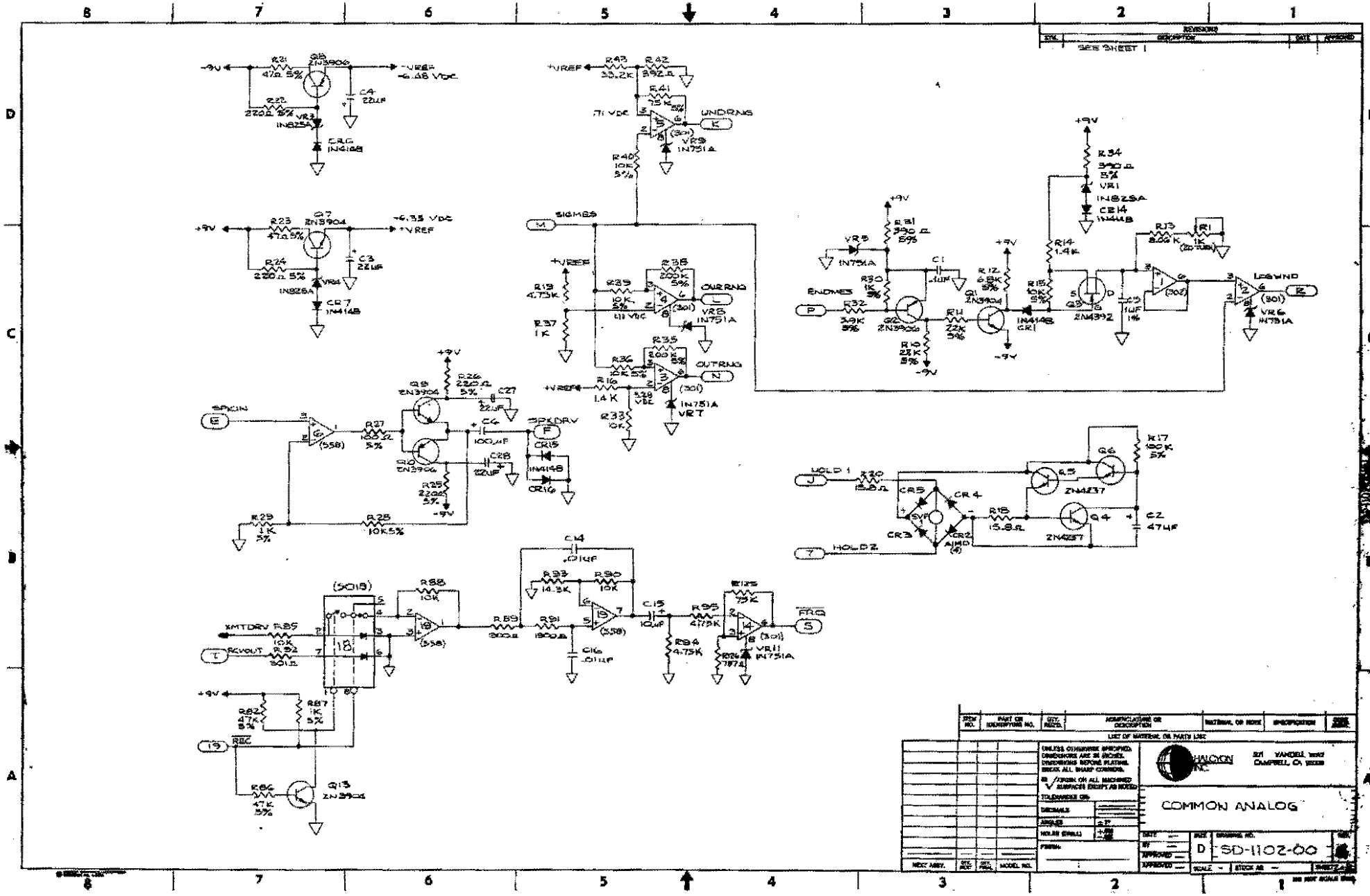
PCB ASSEMBLY– COMMON ANALOG

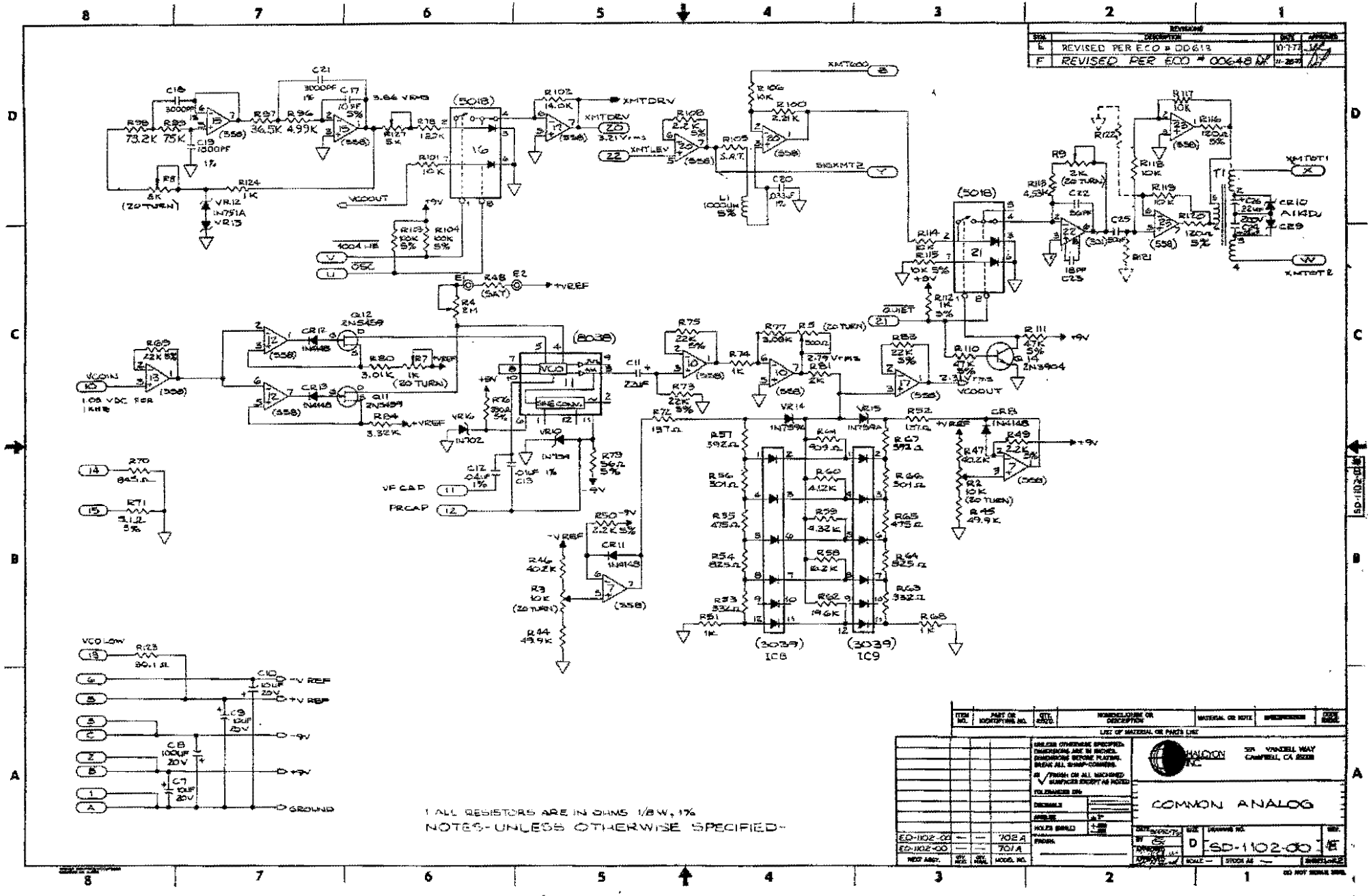
DATE [illegible] | SIZE D | DRAWING NO. ED-1102-00 | REV. C

SCALE 2/1 | STOCK AS 5000 | SHEET 1 OF 1

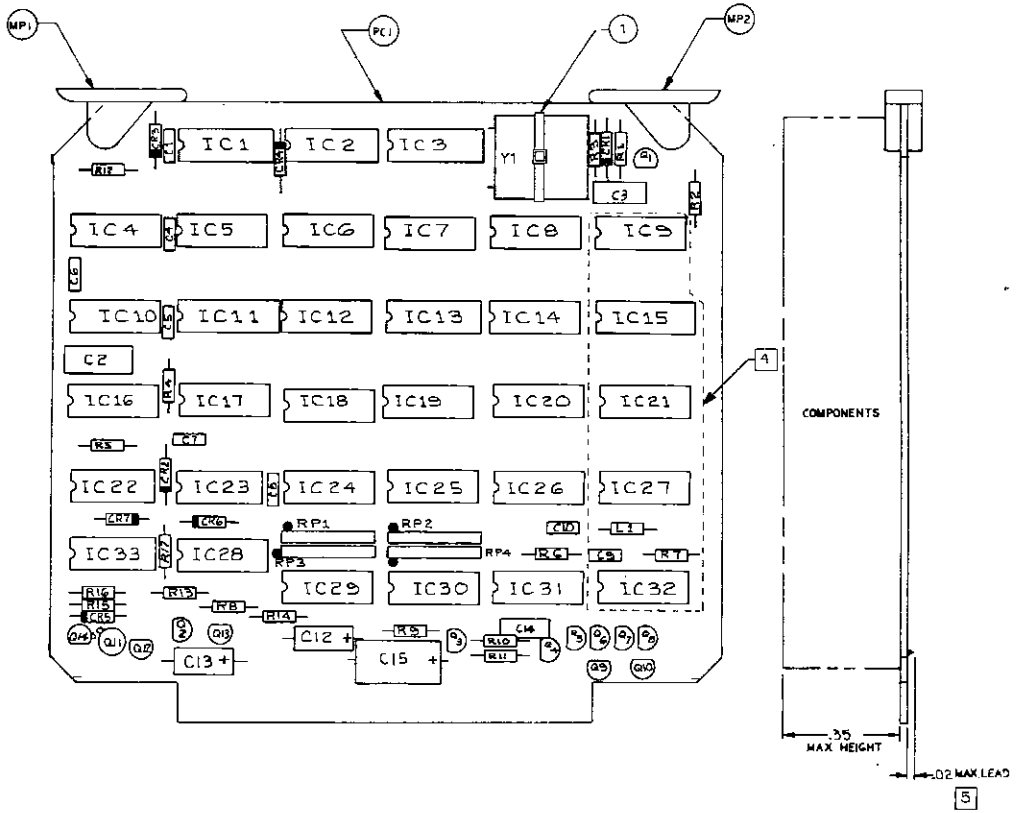
NEXT ASSY. | QTY. NEXT | QTY. FINAL | MODEL NO.

DO NOT SCALE DWG.


SEE SHEET 1
-9V
+VREF
-6.48 VDC
+6.35 VDC
.71 VDC
UNDRNG
SIGMAG
OVRRNG
OUTRNG
ENDMES
LOGWND
SPKIN
SPKDRV
XMTDRV
RCVOUT
REC
FREQ
HOLD 1
HOLD 2
COMMON ANALOG
HALCYON INC.
SD-1102-00


REVISIONS
E REVISED PER ECO # 00613
F REVISED PER ECO # 00648
XMTDRV
XMTLEV
SIGXMT2
VCOOUT
+VREF
-VREF
QUIET
VCOIN
1.06 VDC PER 1 kHz
VF CAP
FRCAP
VCO LOW
+V REF
-9V
+9V
GROUND
IC8
IC9
ALL RESISTORS ARE IN OHMS 1/8 W, 1%
NOTES- UNLESS OTHERWISE SPECIFIED-
COMMON ANALOG
SD-1102-00
SIZE D

REVISIONS				
SYM.	DESCRIPTION		DATE	APPROVED
G	REVISED PER ECO#00817	JKS	2-5-79	



ITEM NO	PART OR IDENTIFYING NO.	QTY REQ'D	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.
1	6002-0110-00	1	TIE WRAP			

LIST OF MATERIAL OR PARTS LIST

5 TRIM LEADS ON CIRCUIT SIDE OF PCB TO WITHIN .02 TO PREVENT SHORTING.

4 DO NOT INSTALL SOCKETS FOR IC9,15,21,27 AND 32.

3. ■ SQUARE PADS DENOTES CATHODE END OF DIODE, POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET.

2. FOR LIST OF MATERIALS SEE 8000-

1. FOR SCHEMATIC SEE SD-

NOTES - UNLESS OTHERWISE SPECIFIED:

NEXT ASSY	QTY NEXT	QTY FINAL	MODEL NO
J-1143-00	1		702A
J-1136-06	1		701A
J-1136-00	1		701A

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS. ⊠ √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED. TOLERANCES ON: DECIMALS ± .XX ± .XXX; ANGLES ± 1°; HOLE SIZE (DRILL) +.005 -.000; FINISH: SEE NOTES

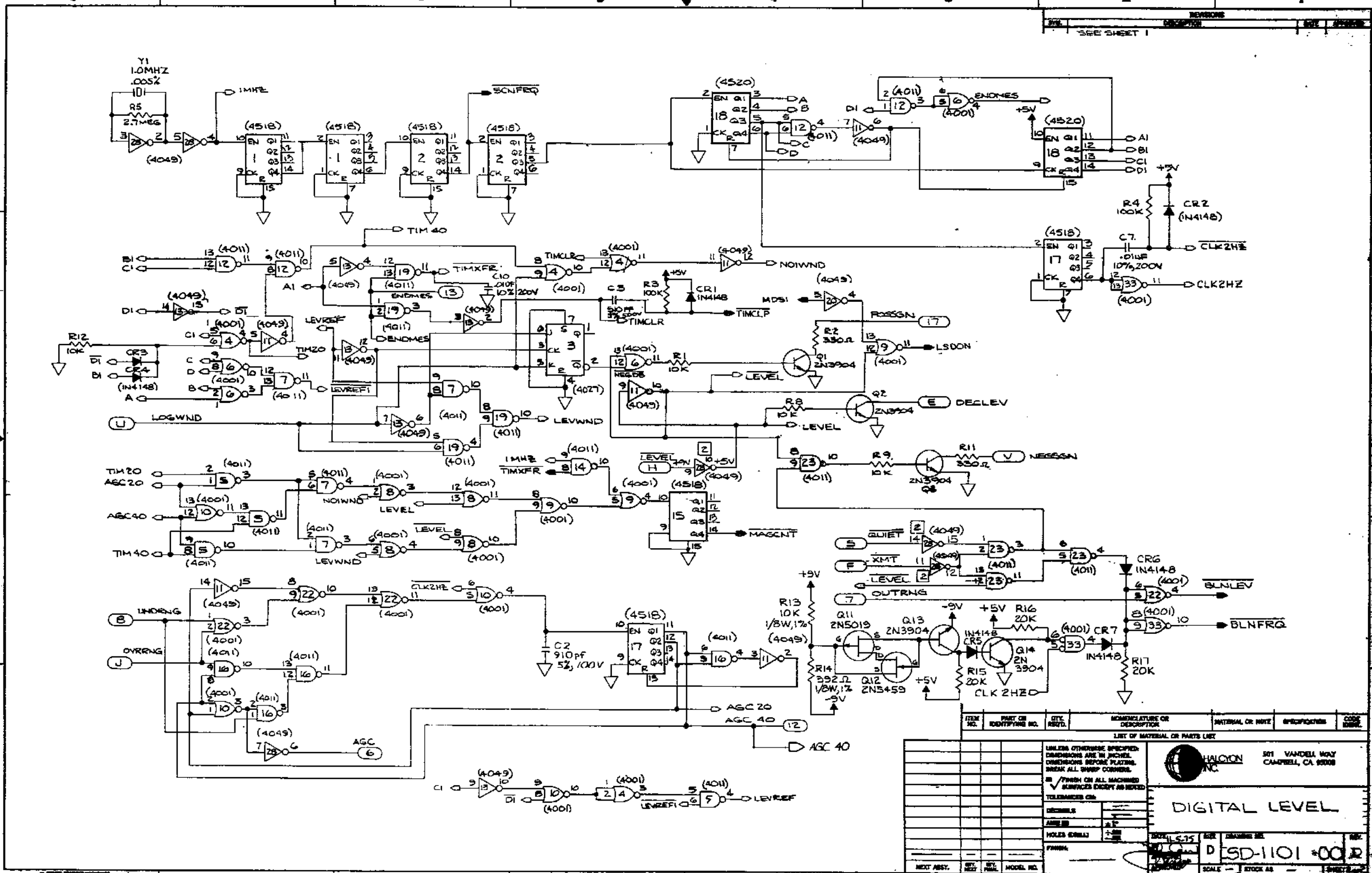
HALCYON INC. 501 — VANDELL WAY CAMPBELL, CA 95008

PCB ASSEMBLY
DIGITAL LEVEL

DATE 2-5-79 | SIZE D | DRAWING NO ED-1101-00 | REV. G

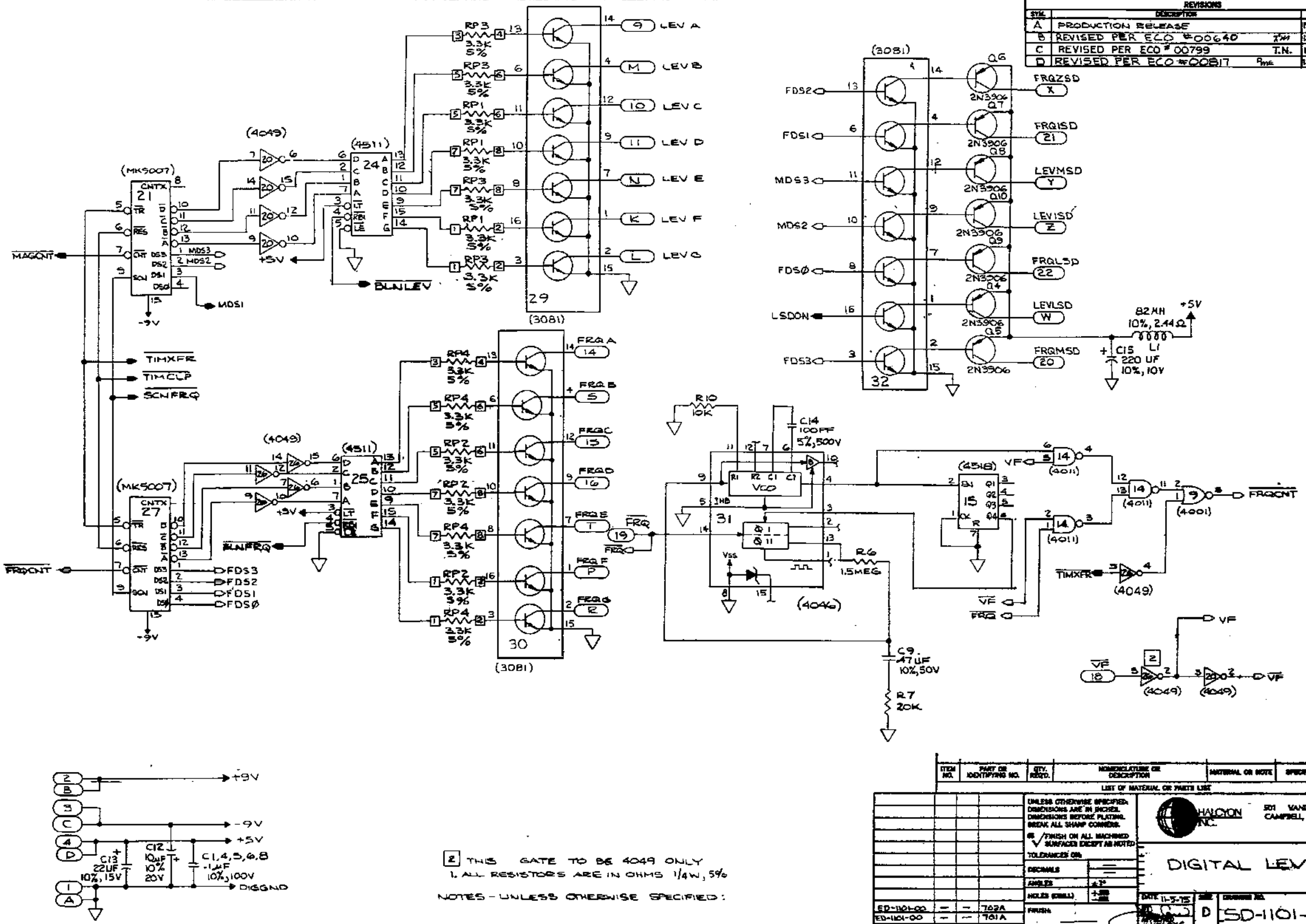
SCALE 2:1 | STOCK AS $000 | SHEET 1 OF 1

DO NOT SCALE DWG



REVISIONS
SEE SHEET 1
Y1 1.0MHZ .005%
R5 2.7MEG
(4049)
1MHZ
SCNFREQ
(4518)
(4520)
ENDMES
CLK2HZ
TIM40
TIMXFR
NOIWND
TIMCLR
TIMCLP
LEVREF
LEVREF1
LEVWND
LOGWND
LSDON
LEVEL
DECLEV
NEGSGN
POSSGN
MAGCNT
TIM20
AGC20
AGC40
UNDRNG
OVRRNG
QUIET
XMT
OUTRNG
BLNLEV
BLNFRQ
AGC
LIST OF MATERIAL OR PARTS LIST
HALCYON INC.
501 VANDELL WAY
CAMPBELL, CA 95008
DIGITAL LEVEL
SD-1101

SYM.	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	11-17-76	
B	REVISED PER ECO #00640	10-11-77	
C	REVISED PER ECO # 00799 T.N.	11-7-78	
D	REVISED PER ECO #00817	12-2-78	



2 THIS GATE TO BE 4049 ONLY
1. ALL RESISTORS ARE IN OHMS 1/4W, 5%
NOTES - UNLESS OTHERWISE SPECIFIED:

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQD.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

NEXT ASSY.	QTY. NEXT	QTY. FINAL	MODEL NO.
ED-1101-00	—	—	762A
ED-1101-00	—	—	761A

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.
FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED
TOLERANCES ON:
DECIMALS
ANGLES ±1°
HOLES (DRILL)
FINISH

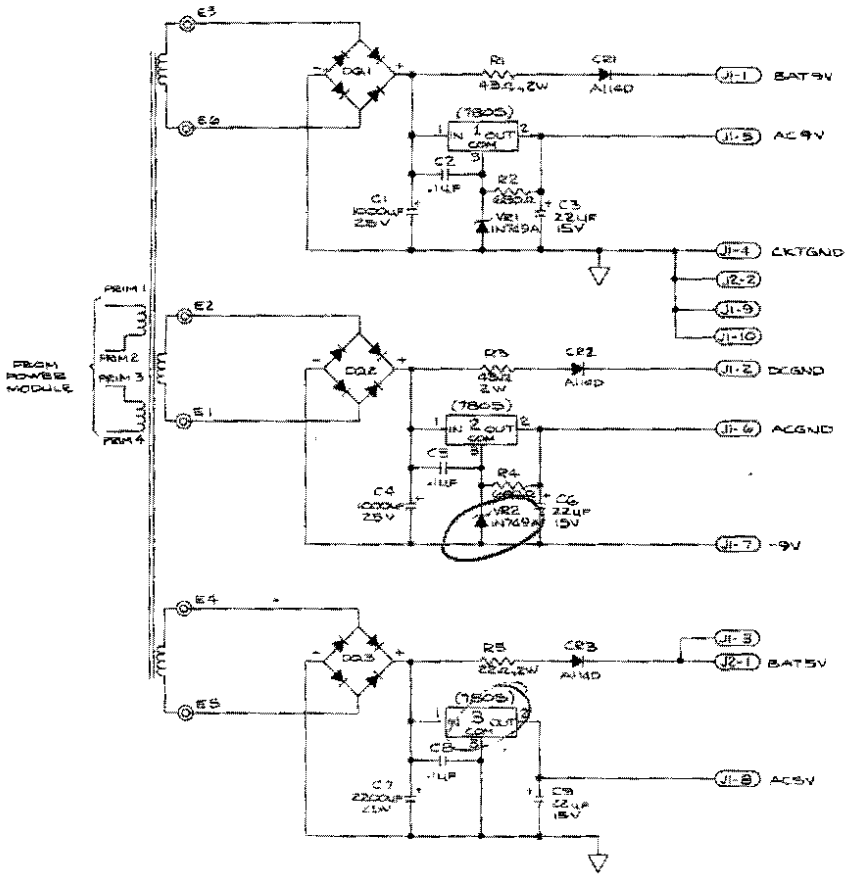
HALCYON INC.
501 VANDELL WAY
CAMPBELL, CA 95008

DIGITAL LEVEL

DATE 11-5-75 | SIZE D | DRAWING NO. SD-1101-00 | REV. D
SCALE — | STOCK AS — | SHEET 1 OF 1

DO NOT SCALE

REVISIONS			
SYM.	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	11-4-76	DS



1. ICS 1, 2 & 3 HAVE HEATSINKS INSTALLED

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CAGE CODE

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

32 √ FINISH ON ALL MACHINED SURFACES, EXCEPT AS NOTED

TOLERANCES ON:
DECIMALS
ANGLES ±1°
HOLES (DRILL) +.005 -.000
FINISH

NEXT ASSY. | QTY. REQ'D. | ITEM NO. | MODEL NO.

HALCYON INC. 321 VANCRIL WAY CAMPBELL, CA 95008

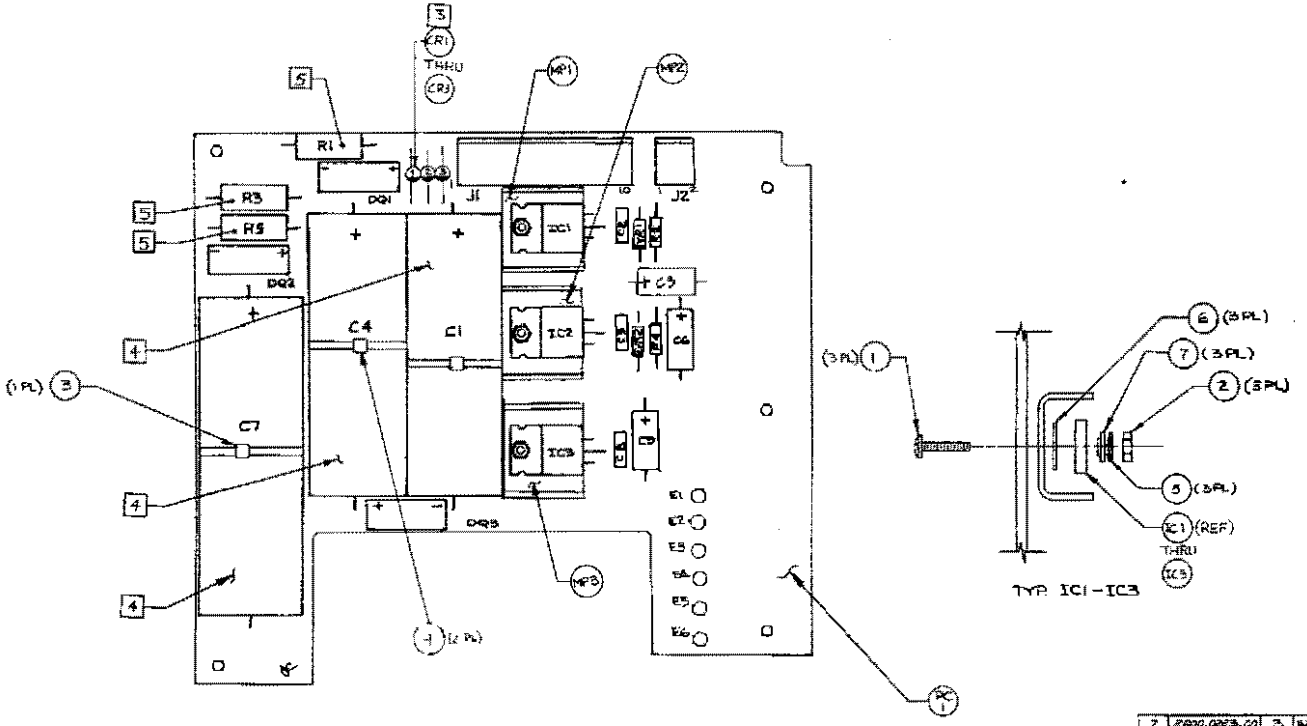
POWER SUPPLY BOARD

DRAWN | SIZE D | DRAWING NO. SD-1104-00 | REV. A

BY | APPROVED | SCALE — | STOCK AS — | SHEET 1 OF 1

DO NOT SCALE DWG.

SYM.	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	9-11-74	P.B.
B	REVISED PER ECO #00610	9-30-75	
C	REVISED PER ECO #00714	5/6/76	
D	REVISED PER ECO # C0655	2-16-78	



ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.
7	2800-0023-00	3	WASHER-SHOULDER, #4			
6	2800-0058-01	3	INSULATOR, #4			
5	2800-0042-00	3	WASHER-SPLIT LOCK #4			
4	6002-0011-00	2	TIE-WRAP			
3	6002-0013-00	1	TIE-WRAP			
2	2800-0028-00	3	NUT-HEX, #4			
1	2800-0124-00	3	SCREW-BH #4-40 X 5/16 LG			

LIST OF MATERIAL OR PARTS LIST

5 INSTALL R1, 3 AND 5 APPROX .125 UP OFF BOARD.

4 SECOND ASSEMBLY C1, C4, & C7.

3 CR1-CR3 TO BE RAISED OFF PCB AT INSTALLATION.

2. FOR LIST OF MATERIALS SEE 8000-1104-00.

1. FOR SCHEMATIC SEE SD-1104-00.

NOTES-UNLESS OTHERWISE SPECIFIED

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

63 √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON: DECIMALS ANGLES ±1° HOLES (DRILL) ±.003

FINISH: SEE NOTES

F.D. 1122 #5	1	--	7044A
S.U. 1122-45	1		101A
NEXT ASSY	QTY REQ'D	SERIAL NO.	MODEL NO.

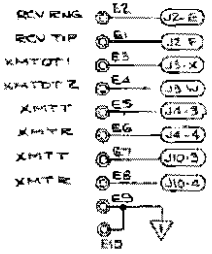
UNION INC. 591 VANDERBILT WAY CAMPBELL CA 95008

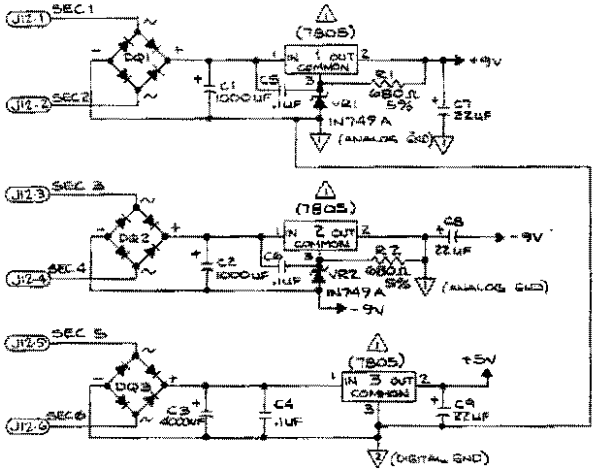
PCB ASSEMBLY-
POWER SUPPLY BOARD

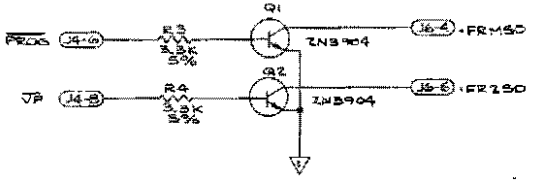
DATE 2-16-78 | SIZE D | DRAWING NO. ED-1104-00 | REV D

SCALE 2X | STOCK NO 8000 | SHEET NO

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE	12/87	DS







2. FOR INTERCONNECTIONS SEE WL-1148-00

⚠1 (1) TWO 3CB MOUNTED ON HEAT SINKS

NOTES - UNLESS OTHERWISE SPECIFIED:

ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

63 √ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED

TOLERANCES ON:

DECIMALS

ANGLES ±1°

HOLES SMALL ±.005

FINISH

NEXT ASSY. | USED ON | MODEL NO.

FALCON INC. 501 YARDELL WAY CAMPBELL, CA 95008

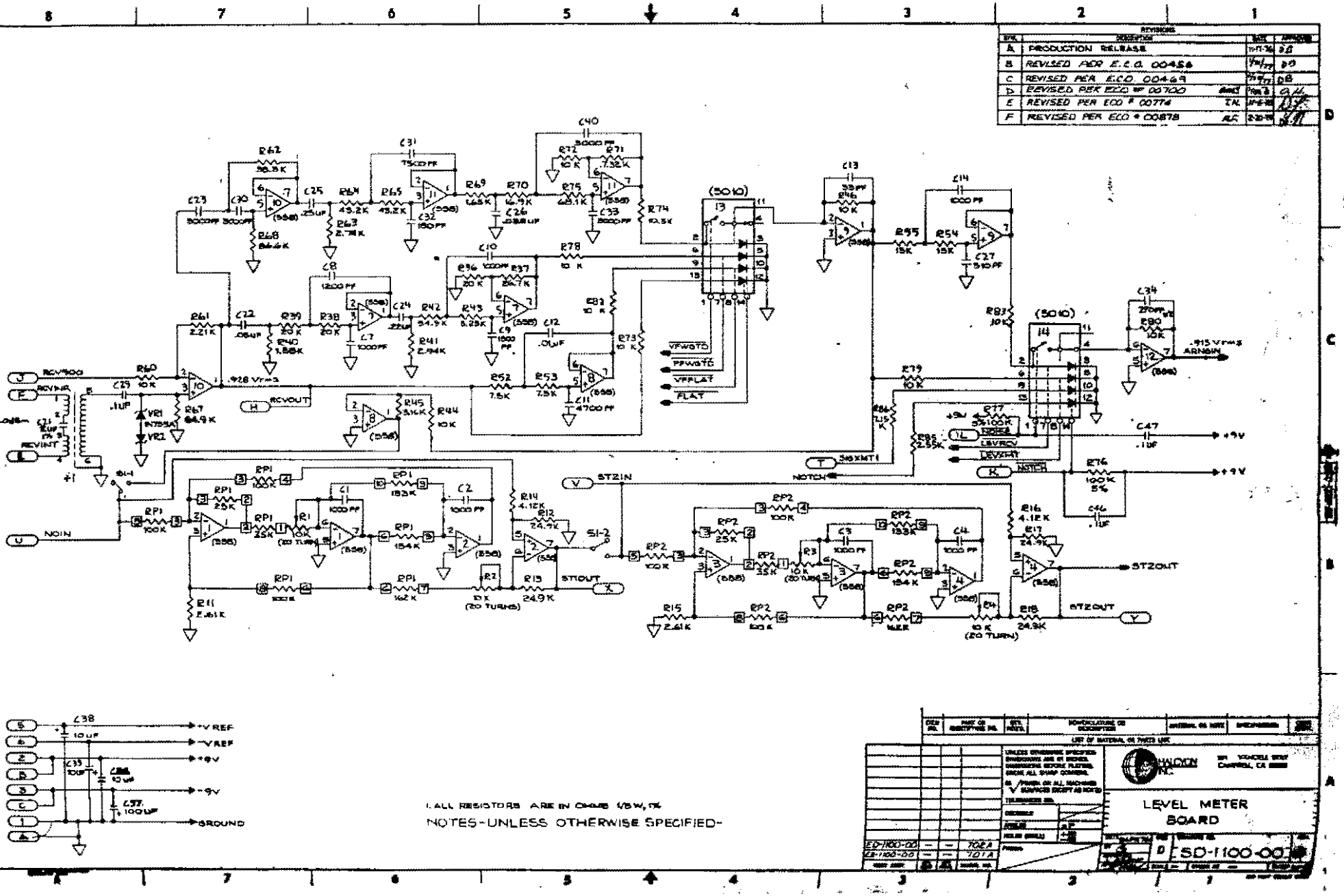
MOTHER BOARD-
702

SIZE D | DRAWING NO. SD-1148-00 | REV. A

DATE 12/87 | DRAWN DS | CHECKED | ENGR APPR. | MFG APPR. | SCALE — | STOCK NO. — | SHEET 1 OF 1

DO NOT SCALE DWG.

MD-1148-00-A


REVISIONS
A PRODUCTION RELEASE
B REVISED PER E.C.O. 00456
C REVISED PER E.C.O. 00469
D REVISED PER ECO # 00700
E REVISED PER ECO # 00774
F REVISED PER ECO # 00878
(5010)
RCVIN
RCVOUT
REVINT
NOIN
STZIN
SI-2
STZOUT
ARNSIN
.915 Vrms
.928 Vrms
+9V
-9V
GROUND
+V REF
-V REF
NOTCH
LEVREV
LEVFWD
VFWDTO
PFWDTO
VFFLAT
FLAT
1. ALL RESISTORS ARE IN OHMS 1/8 W, 1%
NOTES - UNLESS OTHERWISE SPECIFIED -
LEVEL METER BOARD
SD-1100-00

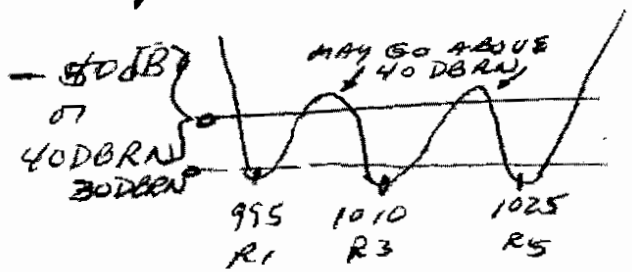
to ADJUST NOTCH:

(4) SET EXT OSC 995HZ 0.0DBM SELECT RCV NOTCH/NOISE
ADJUST R1 ON 1100 BD FOR MIN ↑ 27DBRN

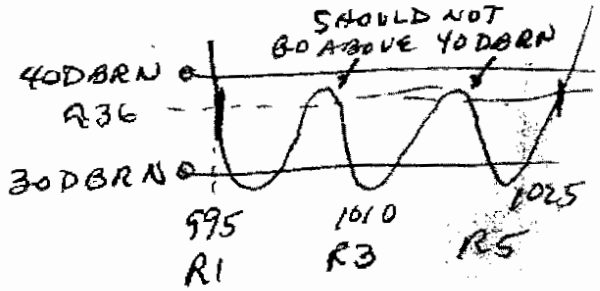
(6) SET EXT OSC 1025HZ 0.0DBM
ADJUST R5 ON 1100 BD FOR MIN ↑ 27DBRN

(C) SET EXT OSC 1010 HZ 0.0DBM
ADJUST R3 ON 1100 BD FOR MIN ↑ 27DBRN

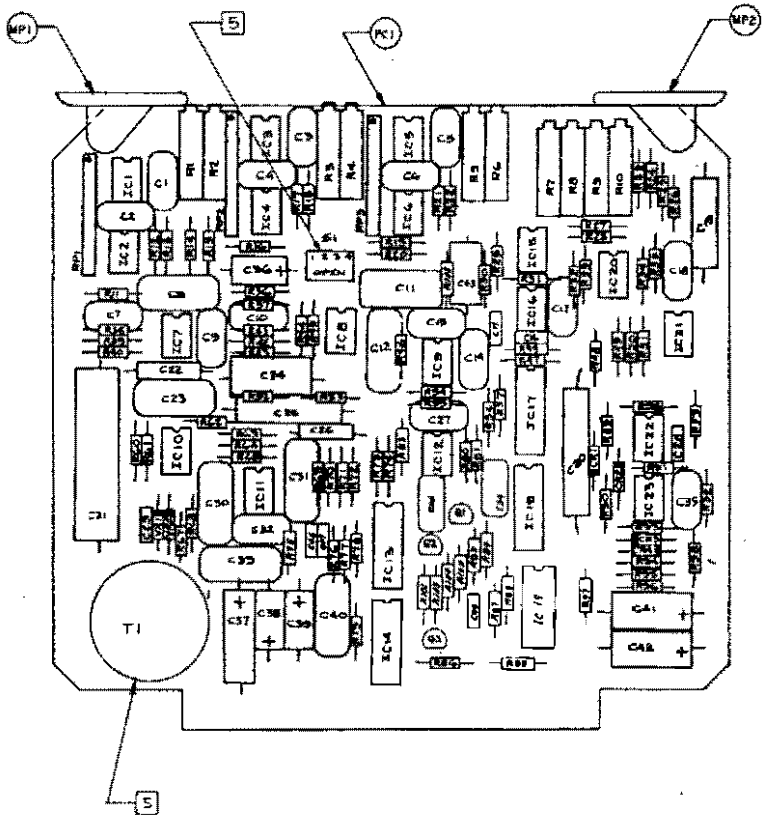
(d) REPEAT a, b, c until all three points require no further adjustment.

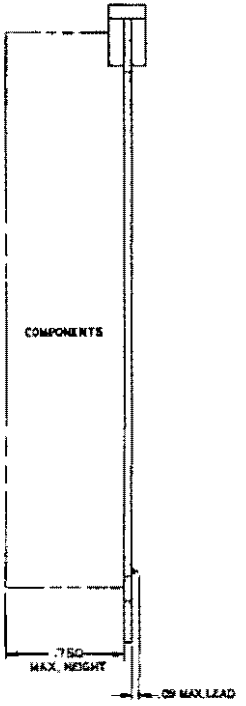


(e) SET OSC FOR 995HZ ADJUST R1 FOR 36 DBRN
(f) " " " 1025HZ " R5 " " " "
CHECK FOR 995 to 1025 ALWAYS
< 40 DBRN



REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED
E	REVISED PER ECO [illegible]	[illegible]	[illegible]





△ T1 & S1 TO BE HAND SOLDERED. DO NOT IMMERSE IN SOLVENT
* FOR PERFORMANCE SPEC. SEE X-1100-GC
1. ■ SQUARE PADS DENOTES CATHODE END OF DIODE, POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET
2. FOR LIST OF MATERIALS SEE 8000-1100-00
1. FOR SCHEMATIC SEE SD-1100-00

NOTES - UNLESS OTHERWISE SPECIFIED:

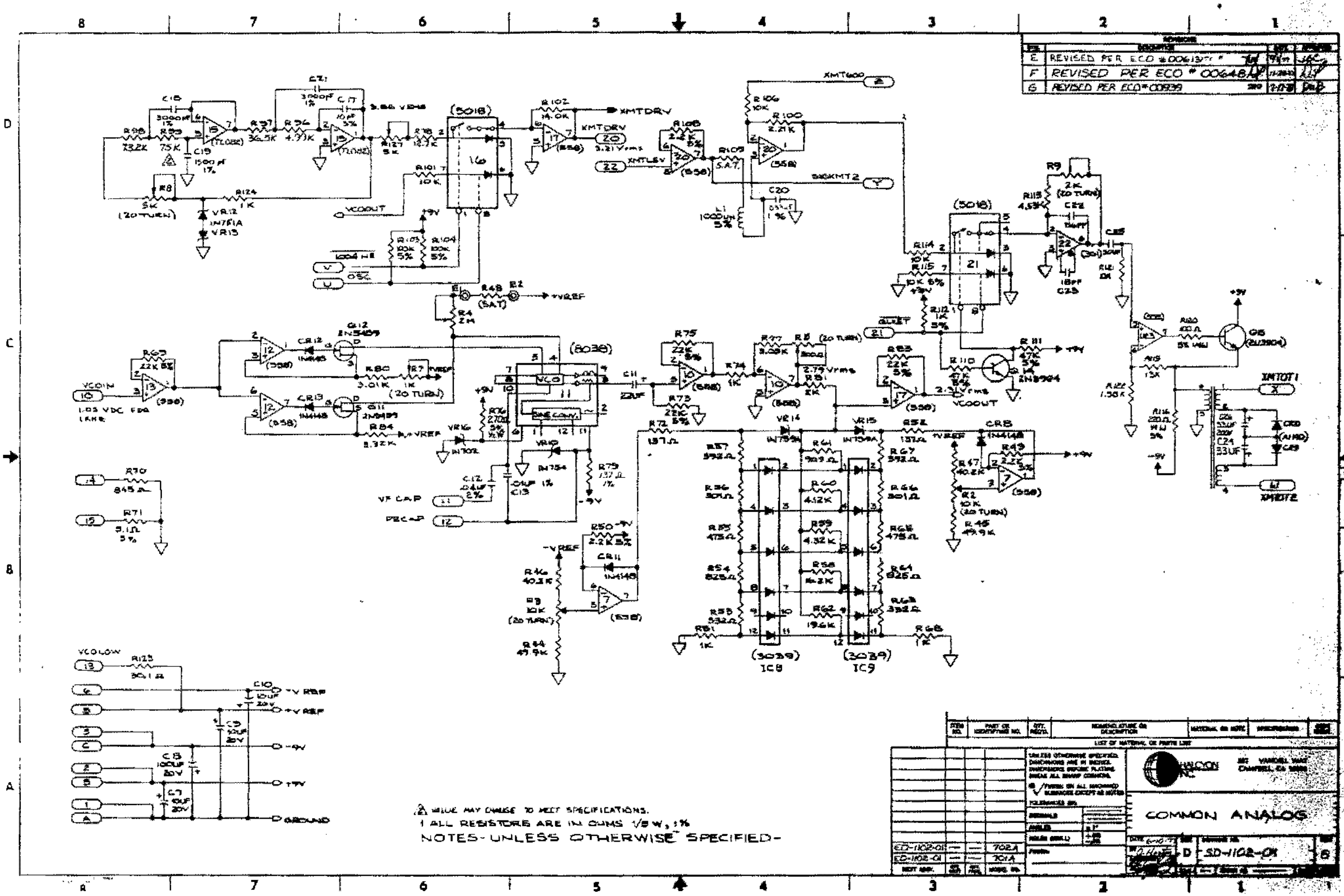
ITEM NO.	PART OR IDENTIFYING NO.	QTY. REQ'D.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR PARTS	SPECIFICATION	CODE IDENT.
			LIST OF MATERIAL OR PARTS LIST			
J-1186-01	1	--	701 A			
J-1151-01	1	--	701 A			
J-1145-01	1	--	701 A			
ED-1100-1F	1		701 A			
ED-1100-1C	1		701 A			
NEXT ASSY	USED ON		MODEL NO.			

UNLESS OTHERWISE SPECIFIED: DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS. ✓ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED. TOLERANCES ON: DECIMALS [illegible] ANGLES ±1° HOLE SIZES +.005 -.001. FINISH: SEE NOTES

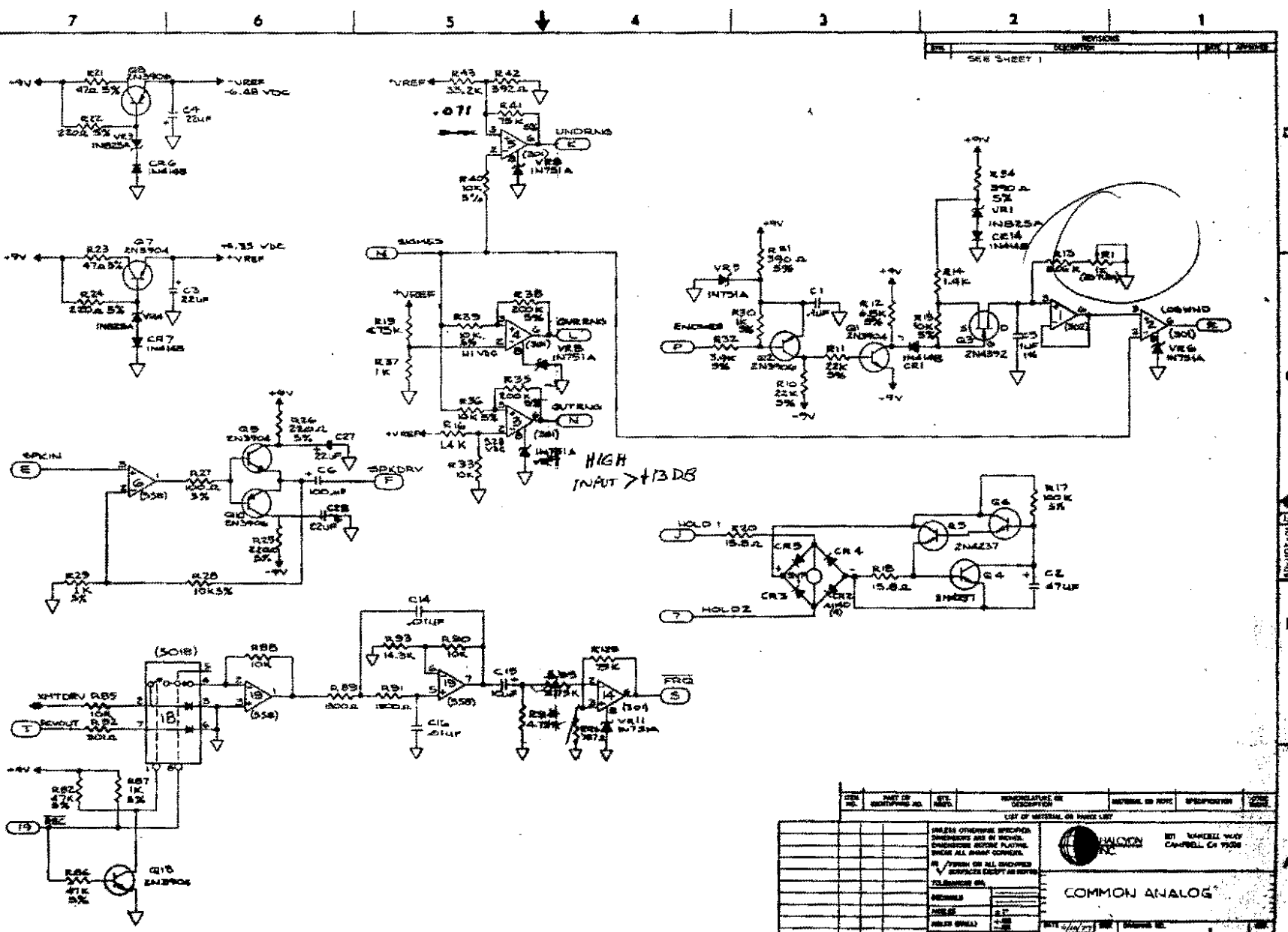
HALCYON INC. 870 — MAXWELL CT. CAMPBELL, CA 95008

PCB ASSEMBLY-
LEVEL METER BD.

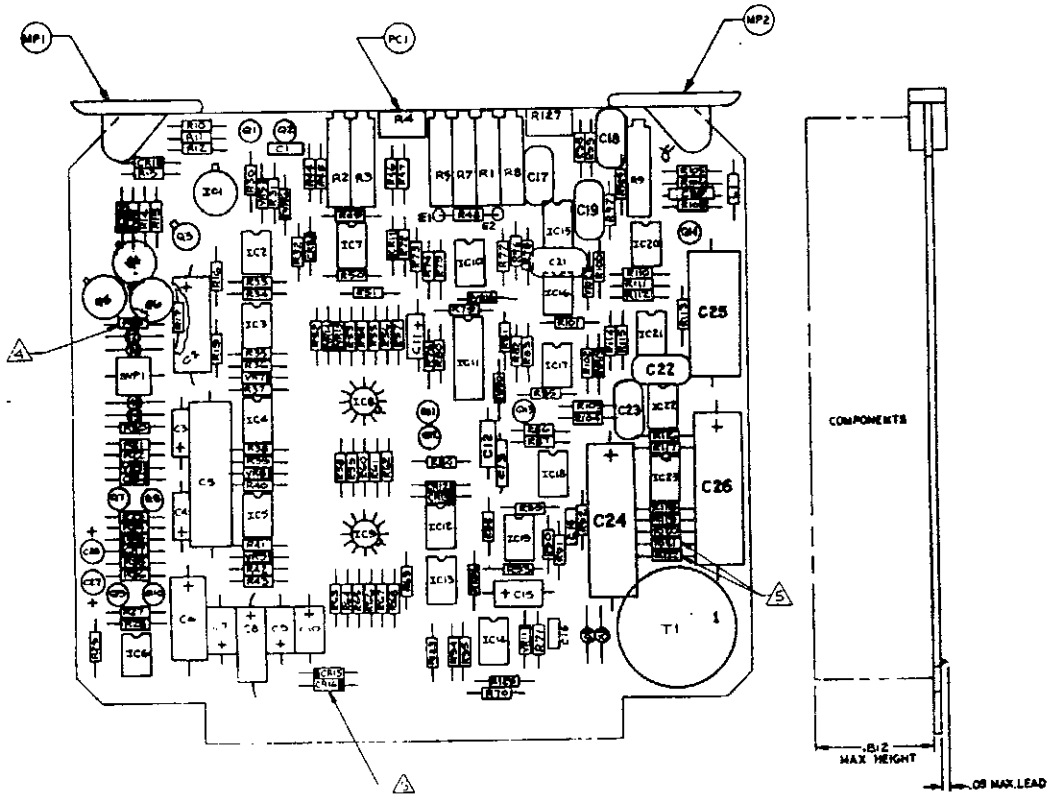
DATE 3-9-79 | SIZE D | DRAWING NO. ED-1100-00 | REV E
BY [illegible] | CHECKED [illegible] | APPROVED [illegible] | SCALE 2:1 | STOCK NO. [illegible] | SHEET NO. 1



E REVISED PER ECO #006137
F REVISED PER ECO # 00648
G REVISED PER ECO # 00939
XMTDRV
XMT600
SIGXMT2
XMTLEV
VCOOUT
1004 HZ
OSC
+VREF
VCOIN
1.05 VDC FOR 1KHZ
(8038)
VCO
SINE CONV.
VF CAP
FBCAP
(3039)
IC8
(3039)
IC9
XMTOT1
XMTOT2
VCOLOW
+V REF
-9V
+9V
GROUND
⚠ VALUE MAY CHANGE TO MEET SPECIFICATIONS.
1 ALL RESISTORS ARE IN OHMS 1/8 W, 1%
NOTES- UNLESS OTHERWISE SPECIFIED-
COMMON ANALOG
SD-1102-01


SEE SHEET 1
HIGH
INPUT >+13 DB
COMMON ANALOG
SD-1102-01

REVISIONS			
ITEM	DESCRIPTION	DATE	APPROVED
A	RELEASED FOR PRODUCTION PER ECO # 00528	4/4/97	WS



⚠5 DO NOT LOAD.

⚠4 INSULATE LEADS OF COMP RIB WITH TEFLON TUBING AND INSURE THAT AN AIR GAP (MIN .03) EXIST BETWEEN Q4, Q5, AND Q6. IF NECESSARY, INSULATE WITH SHRINK TUBING.

3. ■ SQUARE PADS DENOTES CATHODE END OF DIODE, POS END OF CAP, EMITTER OF TRANSISTOR OR GATE OF FET.
2. FOR LIST OF MATERIALS SEE 8000-1102-01
1. FOR SCHEMATIC SEE 80-1102-01

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM NO	PART OR IDENTIFYING NO.	QTY REQ'D	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT

LIST OF MATERIAL OR PARTS LIST

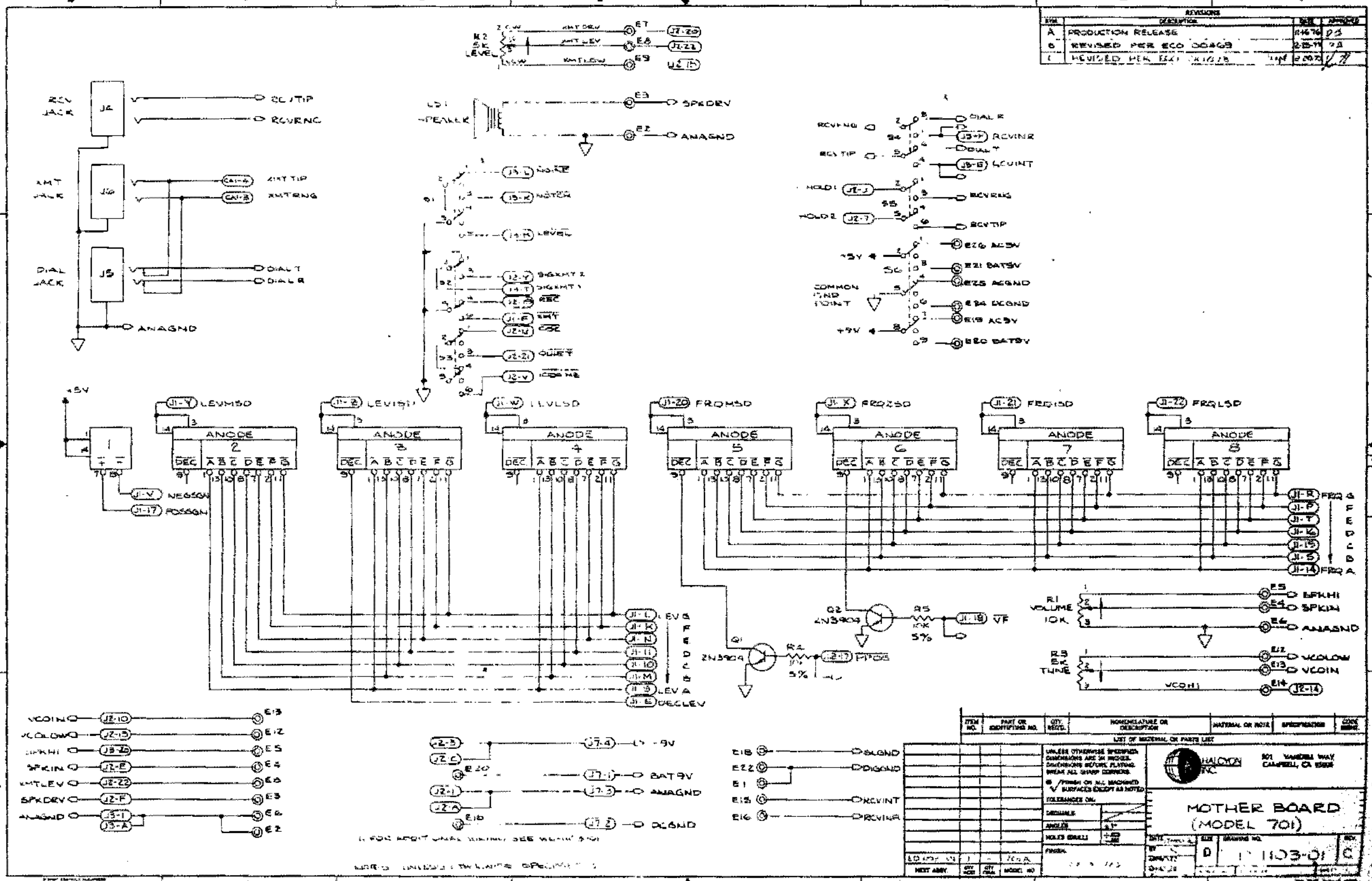
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING APPLY TO ALL FINISH SURFACES. ✓ FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED. TOLERANCES ON: DECIMALS, ANGLES ±1°, HOLES (DRILL) +.005 -.000

HALCYON INC. 501 — CAMPBELL AVE. CAMPBELL CA 95008

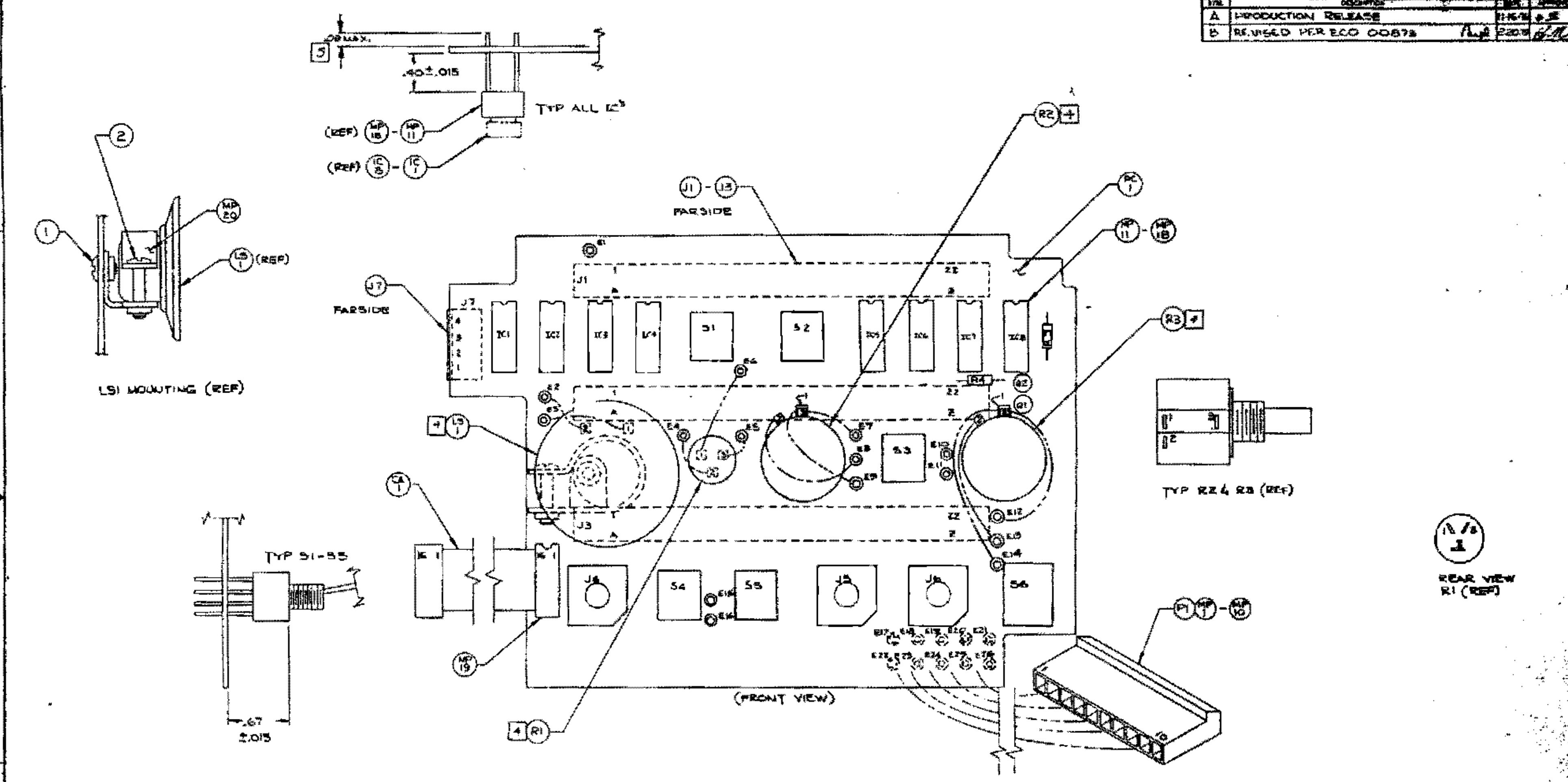
PCB ASSEMBLY- COMMON ANALOG

DATE 4/4/97 | SIZE D | DRAWING NO ED-1102-01 | REV A

ED-1102-01 A


REVISIONS
A PRODUCTION RELEASE
B REVISED PER ECO
C REVISED PER ECO
RCV JACK
J4
XMT JACK
DIAL JACK
J5
ANAGND
RCVTIP
RCVRNG
XMTTIP
XMTRNG
DIAL T
DIAL R
R2 5K LEVEL
XMTDRV
XMTLEV
XMTLOW
LS1 SPEAKER
SPKDRV
ANAGND
NOISE
MOTOR
LEVEL
SIGXMT 1
DIAL R
RCVINR
RCVINT
HOLD1
HOLD2
RCVRNG
RCVTIP
+5V
COMMON GND POINT
+9V
E26 AC5V
E21 BAT5V
E25 AGGND
E24 DCGND
E19 AC9V
E20 BAT9V
+5V
LEVMSD
LEVISD
LEVLSD
FRQMSD
FRQ2SD
FRQ1SD
FRQLSD
ANODE
DEC
A B C D E F G
NEGSGN
POSSGN
FRQ G
F
E
D
C
B
FRQ A
LEV G
F
E
D
C
B
LEV A
DECLEV
Q2 2N3904
R5 10K 5%
VF
Q1 2N3904
R4 10K 5%
R1 VOLUME 10K
SPKHI
SPKIN
ANAGND
R3 5K TUNE
VCOLOW
VCOIN
VCOHI
VCOIN
VCOLOW
SPKHI
SPKIN
XMTLEV
SPKDRV
ANAGND
-9V
BAT9V
ANAGND
DCGND
SIGND
DIGGND
RCVINT
RCVINR
LIST OF MATERIAL OR PARTS LIST
HALCYON INC.
MOTHER BOARD (MODEL 701)
1103-01

SYM	DESCRIPTION	DATE	APPROVED
A	PRODUCTION RELEASE		
B	REVISED PER ECO 00873		



5 MAXIMUM LEAD LENGTH FOR ALL LEADS ON FAB SIDE TO BE .09.

4 FOR MOUNTING AND INSTALLATION ADJUSTMENTS SEE DWG. ED-1122-24

3. FOR SCHEMATIC SEE SD-1103-01

2. FOR LIST OF MATERIALS SEE 8000-1103-01

1. FOR WIRING LIST SEE WL-1103-01

NOTES-UNLESS OTHERWISE SPECIFIED

ITEM NO	PART OR IDENTIFYING NO.	QTY. REQD.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR NOTE	SPECIFICATION	CODE IDENT.

LIST OF MATERIAL OR PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. DIMENSIONS BEFORE PLATING. BREAK ALL SHARP CORNERS.

FINISH ON ALL MACHINED SURFACES EXCEPT AS NOTED.

TOLERANCES ON: DECIMALS; ANGLES ±1°; HOLES (DRILL)

FINISH: SEE NOTES

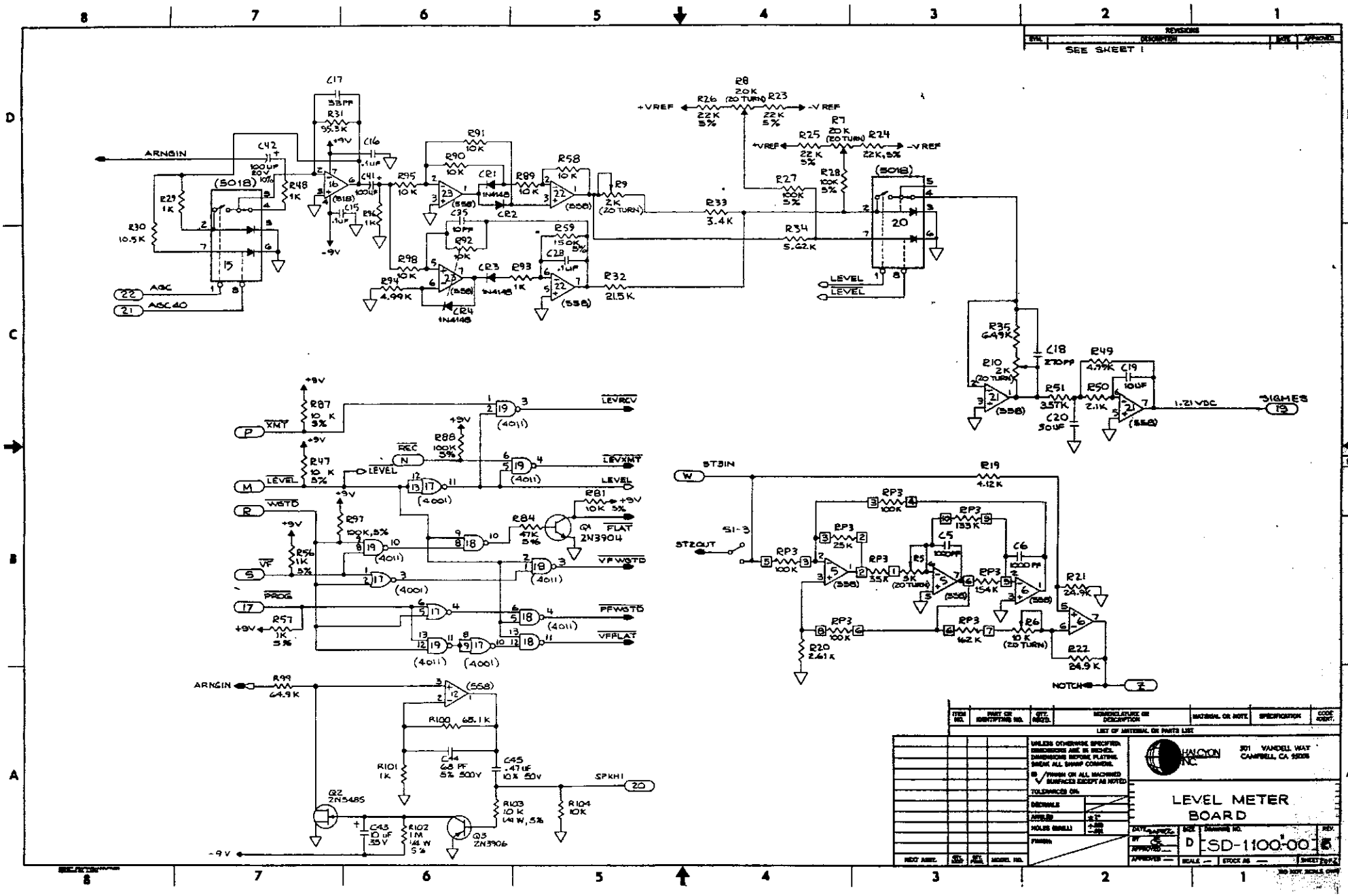
ED 1122-24 — 701A — NEXT ASSY — MODEL NO

INC. CAMPBELL, CA

PCS ASSEMBLY- MOTHER BOARD(701)

SIZE D — DRAWING NO ED-1103-01 — REV B

SCALE 2X


SEE SHEET 1
ARNGIN
AGC
AGC40
LEVEL
LEVEL
+VREF
-VREF
1.21 VDC
SIGMES
XMT
REC
LEVEL
LEVRCV
LEVXMT
LEVEL
WSTD
FLAT
VF
VFWSTD
PROG
PFWSTD
VFFLAT
STBIN
STZOUT
SI-3
NOTCH
SPKHI
LEVEL METER BOARD
HALCYON INC.
301 VANDELL WAY
CAMPBELL, CA 95008
SD-1100-001
D